Pass/Fail Limits -
The Key To Effective Diagnostic Tests

By Harry Dill
Deep Creek Technologies, Inc.

Voice: 410-757-4000 Fax: 410-757-4001 Email: TestDesigner@Compuserve.com

1. Abstract

This paper addresses the application of Pass/Fail limits in discriminating between faulty and fault free circuits. Emphasis is placed on the use of Pass/Fail limits to discriminate among suspected failures in a known faulty circuit during fault isolation and improving test outcome confidence. Analog circuit simulations serve to illustrate failed circuit behavior characteristics and the application of multiple Pass/Fail limits to increase diagnostic resolution.

2. Introduction

One of the most difficult tasks of test synthesis is definition of the criteria that will be used to assign a Pass or Fail outcome to a test. This criteria, more commonly known as Pass/Fail limits, is the principal factor governing key test attributes such as probability of false alarm and probability of detection. Pass/Fail limits also have a profound influence on the diagnostic inferences provided by a test. Ultimately, the Pass/Fail limits influence the quality of diagnostic test sequences. This paper examines new, structured techniques for defining Pass/Fail limits with the objective of creating diagnostic fault trees that isolate failures to smaller ambiguity groups with higher confidence levels.

The experimental data used to derive and support the concepts presented in this paper were formulated from behavioral analysis of a Motor Current Transducer Input Circuit found in a rail transportation car. The circuit schematic is shown in Figure 1. All behavior analyses were prepared using Intusoft's test synthesis tool, Test Designer.

3. Test Definition

There are many different reasons for performing tests. The proof of a hypothesis, evaluation of the performance of a new design under environment extremes, determination of reliability characteristics and verification of fault free performance are but a few. This paper concerns itself with the use of tests to detect and isolate failures in analog electronic circuits of proven design.[1]

All tests used for detection and isolation of faults in an analog circuit are defined by four distinct characteristics - stimuli, observed parameter, point of observation and outcome criteria.

- Stimuli is the environment that the Unit Under Test (UUT) will be exposed to prior to and/or during the observation of a parameter. It can be as simple as a light source to illuminate components during a visual check for discoloration or as complex as thousands of frequency/time division multiplexed RF signals applied to multiple UUT inputs.
- Observed parameter is what is to be measured during the test. Although electronic circuit measurements usually involve voltages, currents, impedances, time and occasionally temperature; measurements may be less quantitative and include odor and color.

- Location of the observation is where on the UUT the observation is to be made. If the observed parameter is component color, the observation point is the location of the component. If voltage is the observed parameter, the observation point is the circuit node where the voltage is of interest.
- Outcome criteria is the standard against which the observation will be compared to determine what information can be inferred from the test outcome. The criteria is usually quantitative in nature and is defined as a "spread" of values. An example of test outcome criteria might be "if a voltage at node X is between 4.5 Volts and 5.5 Volts, the power supply circuit is fault free, otherwise it is faulty." The outcome criteria does not have to be quantitative. The test might be "does the circuit board smell burnt?" In this case, the accuracy of the instrument will vary widely with the tester. Usually only two outcomes are defined for a test - Pass and Fail. However, since Pass and Fail are each associated with some range of an observed parameter and the range of the observed parameter can be subdivided into any number of ranges, the methodologies discussed herein can be easily extended to multiple outcome tests (e.g., Fail Hi, Pass, Fail Lo).

Change any one of these four characteristics and the inferences that can be derived from the test outcome may also change.

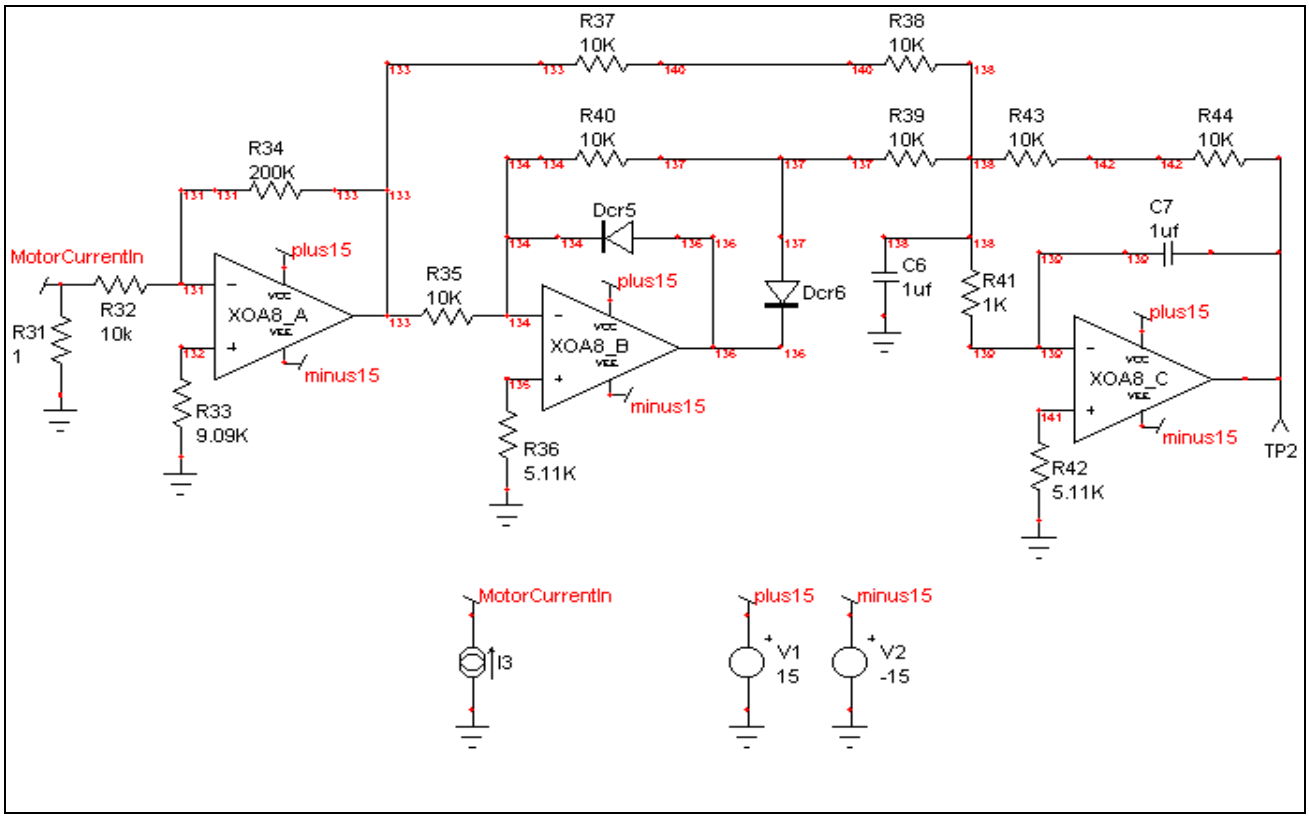

Figure 1 - Motor Current Transducer Input Circuit

4. Test Objectives

The testing objective determines the Pass/Fail limits definition approach. There are many possible testing objectives but the two prominent objectives of industry are *performance verification* and *fault isolation*.

4.1 Performance Verification

Performance verification tests are used to confirm that an assembly is fault free. The most common point of application is on the assembly line as fault isolation and repair is usually not of interest. The objective is to ensure that all assemblies are operational and ready for installation at the next higher level of assembly.

Definition of Pass/Fail limits for performance tests is usually accomplished using one of two methods:

1. the limits are derived from the parametric spread limitations of the inputs at the next higher level of assembly or
2. the tolerances of each of the components of the Unit Under Test (UUT) are used in a Monte Carlo statistical computation to determine limits based on the probability of passing an assembly with a failure in it and failing an assembly with no failure.

Method 1 is the easiest approach *if specifications of the input requirements for the next level of assembly are available.* Often they are not available.

Method 2 can present unnecessary testing challenges as parametric variations of the UUT that result from the use of commonly available components are often much tighter than the design tolerances required by the next higher level of assembly. Consider the example circuit in Figure 1. The resistors each have a tolerance of 5%. The capacitors each have a tolerance of 10%. By performing a Monte Carlo analysis on the example circuit, it is possible to compute the expected value and standard deviation of the voltage at each node.[2] Table 1 shows the mean and 3 sigma voltage values at each node in the example circuit given a Motor Current stimuli of a sine wave voltage having frequency of 71.5 Hz and peak amplitude of 0.3 Volts. Tests have been defined for each node in the circuit. The measured parameter for these tests is mean voltage. Pass/Fail limits have been defined at ±3 sigma. This yields a 1.3×10^{-3} probability of failing any of the tests defined for a known good Motor Transducer Input assembly. Note that the spread between the upper and lower Pass/Fail limit (2 x 3 sigma) is less than 50 mv for 11 out of the 14 tests. This limit spread is below the noise floor of many large automatic test systems (~50mV) and makes 10 of the 14 tests unusable. However, this spread may be much smaller than necessary if consideration is given to the failure mechanisms of the circuit (more on this in the next section). Consider that given no information about failed behavior of the circuit, any measurement outside of the Monte Carlo derived limits indicates that the circuit is faulty. Use of tests having such narrow limits places severe constraints on test instrumentation because instrumentation error and test system noise could easily invalidate the results and identify a fault free UUT as failed.

Table 1 - Node voltage variations due to component parameter in-tolerance variations.

Measurement Node	Mean Voltage	3 Sigma Voltage
131	11.08 uV	82.17 nV
132	-409.9 nV	18.97 nV
133	-38.01 mV	12.55 mV
134	19.45 uV	3.180 uV
135	-230.8 nV	10.53 nV
136	-1.913 V	0.1926 V
137	-1.895 V	0.1890 V
138	115.1 uV	264.6 uV
139	-6.295 uV	2.246 uV
140	-18.99 mV	6.169 mV
141	-229.9 nV	9.336 nV
142	1.926 V	0.2546 V
MotorCurrentIn	1.902 mV	595.8 uV
TP2	3.853 V	0.5098 V

4.2 *Fault Isolation*

Fault isolation tests are used to identify a faulty component within the UUT. The most common point of application is the maintenance and repair facility. The objective is to locate the faulty component, make repairs, and return the UUT to service.

Fault isolation tests offer a broader latitude for limit setting as their "Pass" outcome does not necessarily require that there is no failure in any UUT component involved in the generation of the observed parameter. As a simple illustration, Figure 2 shows the spread of measurements at node 138 of the example circuit when there are no failures. The X-axis of Figure 2 has the units of Volts and has been expanded around the 4.75 sigma "no fault" range to illustrate just how small this range is. Plotted together with this "no failure" measurement spread are the nominal values of node 138 voltage for the predefined failure modes. The four failure modes contained within the "no fault" range are not detected by this test regardless of the Pass/Fail limits. This example uses the Test Designer failure mode defaults of 100 megohms for open resistors, open diodes and open capacitors, and 0.1 ohms for shorted capacitors. Figure 2 also shows a single Pass/Fail limit that has the objective of isolating failure mode R44 Open from some (but not all) of the other suspect failure modes. If the test fails (i.e., is below the limit), failure mode R44 Open may have been the culprit; if the test passes, there is high confidence that failure mode R44 Open is not a problem. Note that the pass region for the fault isolation test shown in Figure 2 encompasses all of the expected no fault range of values (2 x 4.75 sigma) as well as a large portion of the fail range of voltages for the circuit shown in Figure 1. If the outcome is defined as Fail for voltage observations below the criterion and Pass for observations above the criterion we

can use the Fail outcome to isolate R44 Open, R43 Open, R36 Open, XOA8_C stuck at minus 15, XOA8_C Open and XOA8_B stuck at minus 15 from the other 25 failure modes in the circuit.

Placing a Pass/Fail limit at the -0.75 Volt level for the example circuit offers several advantages over placing Pass/Fail limits at the 4.75 sigma voltage levels about the mean.

- The test outcome is more reliable because the spread between the upper and lower Pass/Fail limits is much greater than the noise floor of the test system. Actually, for this example there is no upper limit; as long as the noise floor of the test system plus the lowest expected measurement in the "Pass" range is greater than the Pass/Fail limit, the probability of false failures due to system noise will be low.
- The test inferences are more reliable. Consider the case of ±3 sigma Pass/Fail limits for the example circuit. Figure 2 shows 19 failure modes with corresponding node 138 voltages within 161 millivolts of the lower Pass/Fail limit. Five of these failure modes have associated node 138 voltages less than 1millivolt from the lower limit. Because each circuit card in a population has its own unique set of tolerances, UUTs having node 138 voltages at the high end of the distribution for the case of no failures may shift the X-axis of Figure 2 sufficiently far to the left relative to the fixed Pass/Fail limits to make several of the 19 failure modes undetectable. The -0.75 Volt Pass/Fail limit shown in Figure 2 has a much higher immunity to this inference uncertainty. There is a 500 millivolt "buffer zone" on both the high and low sides of the limit. If the test fails, there is high confidence that the culprit is R44 Open, R43 Open, R36 Open, XOA8_C stuck at minus 15, XOA8_C Open or XOA8_B stuck at minus 15. If the test passes there is high confidence that the culprit is one of the other 25 failure modes or the circuit contains no failures.
- Tests having "tailored" failure mode inferences can be synthesized by moving the Pass/Fail limits to the appropriate position on the measurement range. For example, consider a Pass/Fail limit placed at the +1.5 Volt level in Figure 2 and assign an outcome of "Fail" to the test if the observed parameter is greater than this limit. By doing nothing more than moving the Pass/Fail limit from -0.75 Volts to +1.5 Volts, the failure mode inference has been changed from R44 Open, R43 Open, R36 Open, XOA8_C stuck at minus 15, XOA8_C Open and XOA8_B stuck at minus 15 to XOA8_C stuck at plus 15.

5. UUT Behavior Characterization

In order to take advantage of failure information during the development of effective performance and fault isolation tests, the behavior of the circuit must be characterized in terms of what parameters will be observed at each observation point for each failure mode. Pass/Fail limits can then be assigned to achieve the desired fault detection (e.g., inference) characteristics. Until recently, this task was computationally intractable for all but the simplest of circuits. With computer clock speeds now exceeding 300mHz, simulation has become a viable solution.

5.1 Failure Free UUT Behavior

There are three views of failure free UUT behavior - each correct when taken in context.

1. *UUT meets all manufacturer's performance specifications.* For example, a DC Power Supply may have requirements of 5±0.001 Vdc for a load of 1 amp and an input of 120±15 Vac at 60 Hz.
2. *UUT meets all performance requirements for the next higher level of assembly.* A digital control circuit with discrete outputs may require power of 5±0.5 Vdc for a load of 250 ma and an input voltage of 120±15 Vac at 60 Hz. Leaky filter capacitors may render the DC Power Supply cited in view 1 incapable of meeting manufacturers specifications. That same "failed" Power Supply may be fully functional in the context of the digital control application.
3. *A set of tests designed to detect all UUT failures in a predefined UUT failure universe show that no failures in that universe exist.* This view is often used by test engineers when designing fault isolation tests that have measurements at observation points for which no manufacturer's specifications exist and the measured parameters are not tightly coupled to the requirements at the next higher level of assembly.

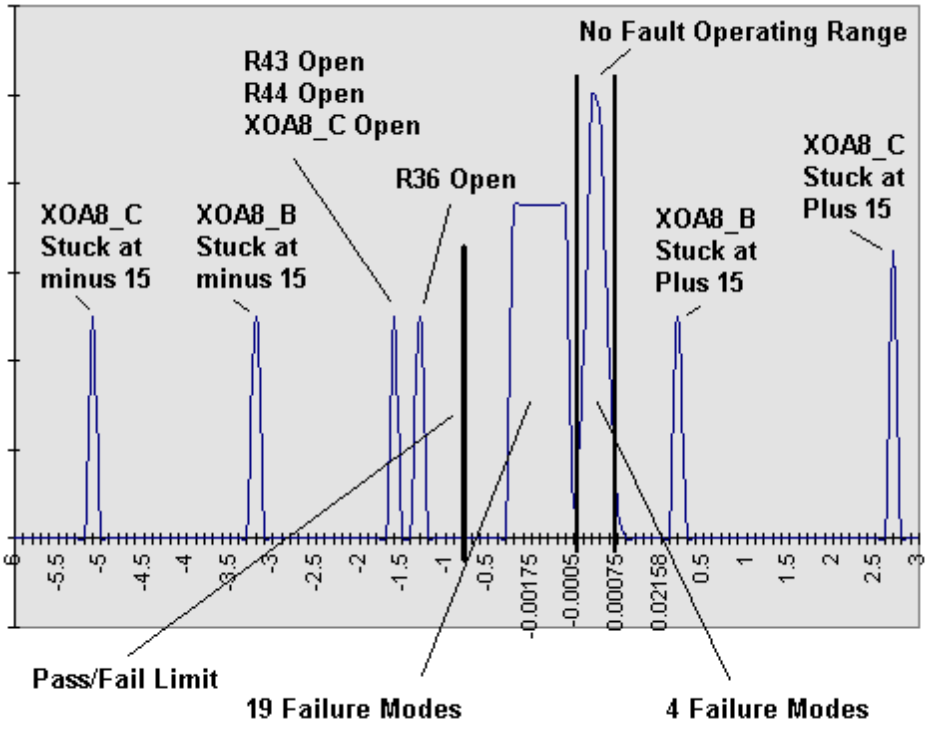

Figure 2 - Node 138 Voltages For Failure Modes and No Failure

The approach presented here combines these three views by testing UUT outputs to the next higher level of assembly requirements if they are known and the manufacturer's specifications if the next higher level of assembly requirements are not known. The view 3 approach is particularly useful when the available instrumentation is not capable of performing measurements

within the UUT manufacturer's tolerances and the next higher level of assembly requirements are unknown.

Figure 3 shows the TP2 output of the example circuit along with the nominal expected voltage for each failure mode. Also shown in the figure are 4.75 sigma Pass/Fail limits. These limits represent a 1.62 Volt spread. To illustrate the use of failure mode behavior information for increased test outcome confidence, consider the hypothetical case where the voltage at TP2 is to be measured with an instrument having a 1.5 volts peak to peak (mean) noise floor of Gaussian distribution. With Pass/Fail limits set at 1.62 Volts, the instrumentation noise would cause the test outcome to occasionally Fail when in fact the TP2 voltage is within the 1.62 Volt Pass range. This incorrect fail outcome is commonly known as a false alarm. (The frequency of false alarm is a function of the noise characteristics.) Now consider the case when the Pass/Fail limit spread is increased to 4 Volts (±2 Volts about the mean). An examination of Figure 3 shows that there is no affect on the fault detection characteristics of the test. However, the number of false alarms for this test should decrease as the Pass/Fail limits are now significantly further away from the mean of the instrument noise floor voltage.[3]

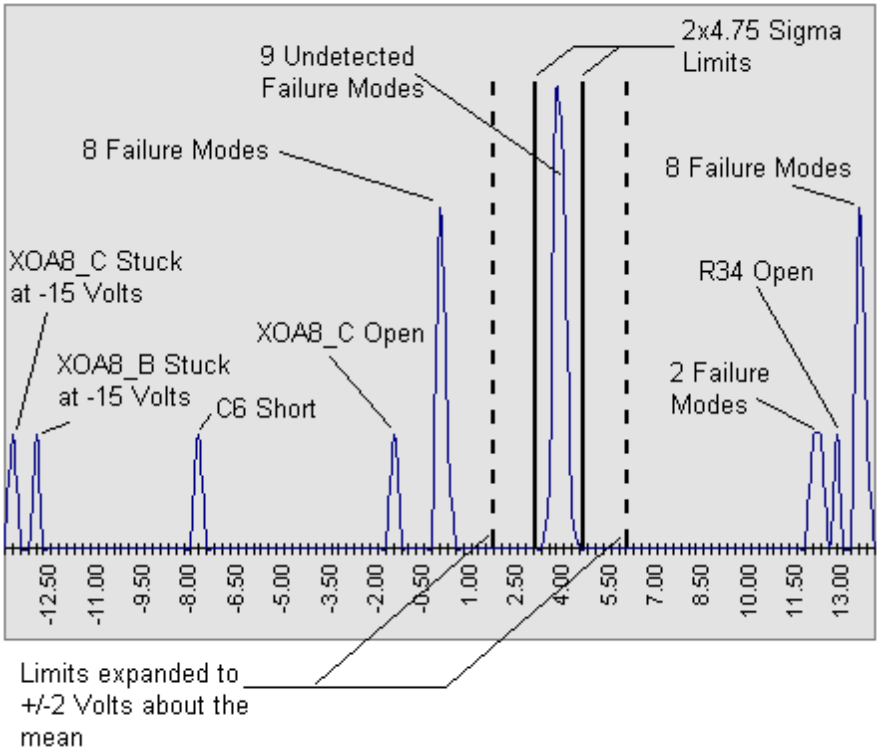

Figure 3 - Failure information shows limits can be expanded without affecting test results.

5.2 Failed Behavior

Computation of failed circuit behavior requires knowledge of component failure mode parameters. For purposes of this paper, component failure mode definitions have been extracted from the CASS Red Team Package and failed component parameters have been assigned to every

component in the example circuit (e.g., open resistor is 100 megohms, shorted transistor collector-emitter is 0.1 ohm, etc.). This set of failures is known as the failure universe and represents the set of conclusions (with the addition of No Fault) from which we must draw during fault isolation.

Figure 2 shows the failed voltage measurement to be expected at node 138 of the example circuit for each failure mode parameter defined in the fault universe. Note that we are defining a specific value for the component failure mode parameter in this analysis. In the real world, a spread of failed values is a more realistic assumption, however, a Monte Carlo analysis around every failure mode parameter is computationally prohibitive. Therefore, when capturing failed behavior for use in setting test limits, it is incumbent upon the test engineer to examine each failure mode definition and determine the most suitable parameter(s) for failure mode characterization. Some failure modes drive circuit parameters into stable states over wide ranges of component failure parameters. Other failure modes drive circuitry into non-linear operational regions that make the circuit ultra sensitive to variations in the parameter used for the failed component. Fortunately, modern circuit simulators such as Test Designer automate analysis of component parameter variations and facilitate selection of appropriate component failure parameters.

An interesting sidenote: Experience with the Test Designer simulator has shown that for some failure modes, a circuit will exhibit instability for the stimuli of Test A and the failed circuit behavior is unpredictable; yet, for the same failure modes, circuit stability is excellent for the stimuli provided by Test B and the failed circuit behavior is highly predictable. This argues for *ordering tests to eliminate failure modes from consideration that cause circuit instabilities in subsequent tests.* This is a subject for future investigation.

6. Setting Pass/Fail Limits

The previous sections show how individual failure modes induce specific circuit behavior that can be characterized for a given test stimuli. This information can be captured in tests and used to decrease the granularity of fault isolation and increase the ability to reliably discriminate among failure modes. This section of the paper describes the creation of multiple tests that use exactly the same stimuli, measured parameter and measurement location. These tests differ *only* in their respective Pass/Fail limits definition.

6.1 Binary Tests

Binary tests are defined as tests having an upper Pass/Fail limit and a lower Pass/Fail limit. If the measured parameter is greater than the lower limit and less than the upper limit, the test outcome is defined as Pass, otherwise, the outcome is Fail. This is the conventionally implemented test type for performance testing. It assumes that if the outcome is Pass, then no failure mode was detected.

Now let's take an unconventional view of the binary test. Figure 4 shows a graph of the TP2 voltage versus failure modes for the example circuit. Note that the Pass/Fail limits have been intentionally set such that the Pass region (e.g., the range of parameters between the lower and upper limit) encompasses parameters expected for nine failure modes but excludes the parameter range for No Fault. Also note that the Fail regions (e.g., measurements greater than the upper

limit and less than the lower limit) include not only expected measurements corresponding to failure modes but also the range of parameters defined for No Fault. Thus, by setting limits, we have defined the inferences (e.g., fault detection characteristics) that can be made from the Pass outcome (nine failure modes) and the Fail outcome (22 failure modes plus No Fault) of this test. By moving the limits around in this manner, the test engineer can tailor the detection characteristics of the test to the fault isolation requirements. Applying this technique, it is possible to design a set of tests using a single set of stimuli and a single measurement at a given point, that have enhanced fault isolation characteristics over binary tests that center Pass/Fail limits around the No Fault parameter range.

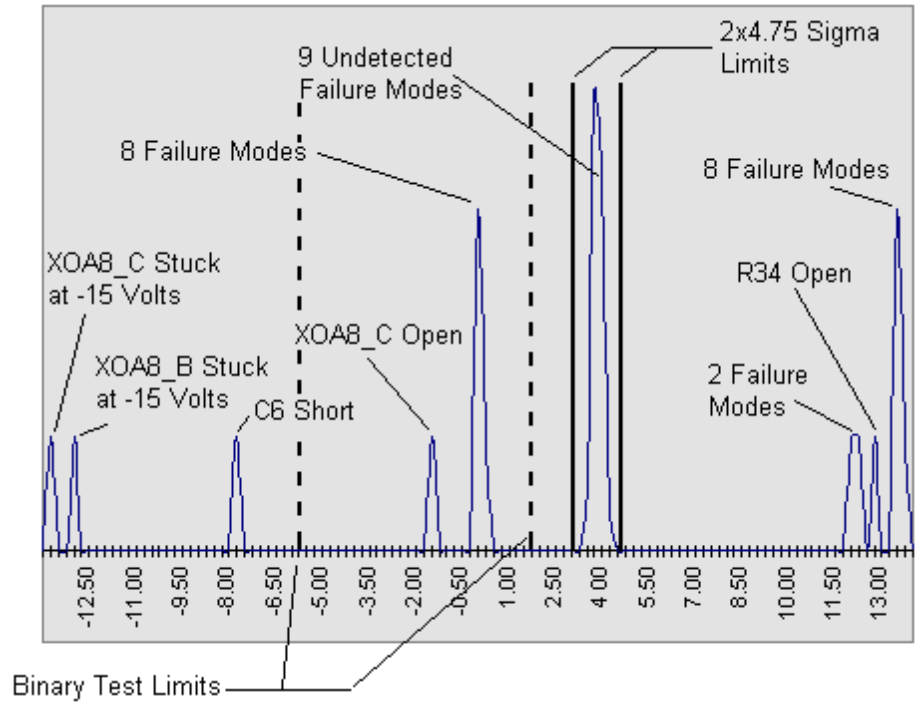

Figure 4 - Binary test Pass/Fail limits set for specific fault detection characteristics.

6.2 Tertiary Tests

Tertiary tests are an extension of binary tests in that they consider only one Pass/Fail limit at a time. The measured parameter can be greater than the upper limit (Test Outcome is Fail Hi), less than the lower limit (Test Outcome is FailLo), or within the Pass region bounded by the lower and upper limits.

The inferences that can be made from the tertiary test are:

1. If the test outcome is Fail Hi then the failure must be in the set of failures associated with the parameters above the upper limit
2. If the test outcome is Fail Lo then the failure must be in the set of failures associated with the parameters below the low limit.
3. If the test outcome is within the Pass region, the failures associated with parameters above the upper limit and below the lower limit are eliminated from consideration.

The Pass/Fail limits defined for the binary test shown in Figure 4 can also be used for a tertiary test. In this example, if the test has an outcome of FailLo then three failure modes are inferred - C6 Short, XOA8_B Stuck at -15 Volts and XOA8_C Stuck at -15 Volts. If the test outcome is Pass, XOA8_C Open 8 other failure modes and No Fault are inferred. If the test outcome is Fail Hi, 20 failure modes are inferred.

7. Summary

The parameters that characterize a failed circuit component govern the behavior of the circuit containing the failure. Knowledge of circuit response to component failure modes can be used during the synthesis of diagnostic tests to control the inferences that can be made for each test outcome. The specific mechanism is the selection of Pass/Fail limit criteria.

Knowledge of circuit response to component failure modes is useful for increasing the reliability of test outcomes. By setting Pass/Fail limits in regions away from expected failed parameter values and no failure parameter values, the probability of false alarm is reduced.

Simulation is an effective tool for reducing workload while characterizing circuit response to each failure mode. It is useful for both identifying stable failure response and also identifying test stimuli that can eliminate circuit instabilities associated with some failure modes.

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[1] A. Boros, Electrical Measurements In Engineering, ELSEVIER, 1985, pp. 29-40.

[2] John Staudhammer, Circuit Analysis By Digital Computer, Prentice-Hall, Inc., 1975, pp. 292-307.

[3] W. Bolten, Electrical and Electronic Measurement and Testing, Longman Scientific and Technical, 1992, pp. 1-21 and 235-246.