AND8078/D

A Simple Low-Cost Non-Isolated Universal Input Off-Line Converter

Prepared by: Roland Saint–Pierre
Field Applications Engineer

ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

Switch–mode off–line power conversion typically entails a means of galvanic isolation from primary to secondary. In most instances it includes a step–down high frequency transformer, which aids in the voltage conversion necessary from the high DC bulk voltage generated from the bridge rectifier to the lower output DC voltage required by the end application. If isolation is not a requirement of the application, in which safety can be insured by mechanical means, the additional cost of the transformer and opto–coupler can be saved. The circuit describe herein is proposed as a simple and low cost means to convert the AC mains voltage to a lower DC voltage which may be used in a variety different applications which include a pre–regulator for a linear voltage regulator.

Circuit Description

The circuit shown below is a very low cost, universal AC input, non–isolated converter employing a buck–boost topology. The simple half–wave rectified AC input provides a DC voltage to the bulk capacitor (C1), which is then converted, to the semi–regulated DC voltage required on the output. For this power level an LC π–filter was chosen to meet conducted EMI requirements. This example describes the design and analysis of a converter providing ~8.0 VDC at 0.4 A.

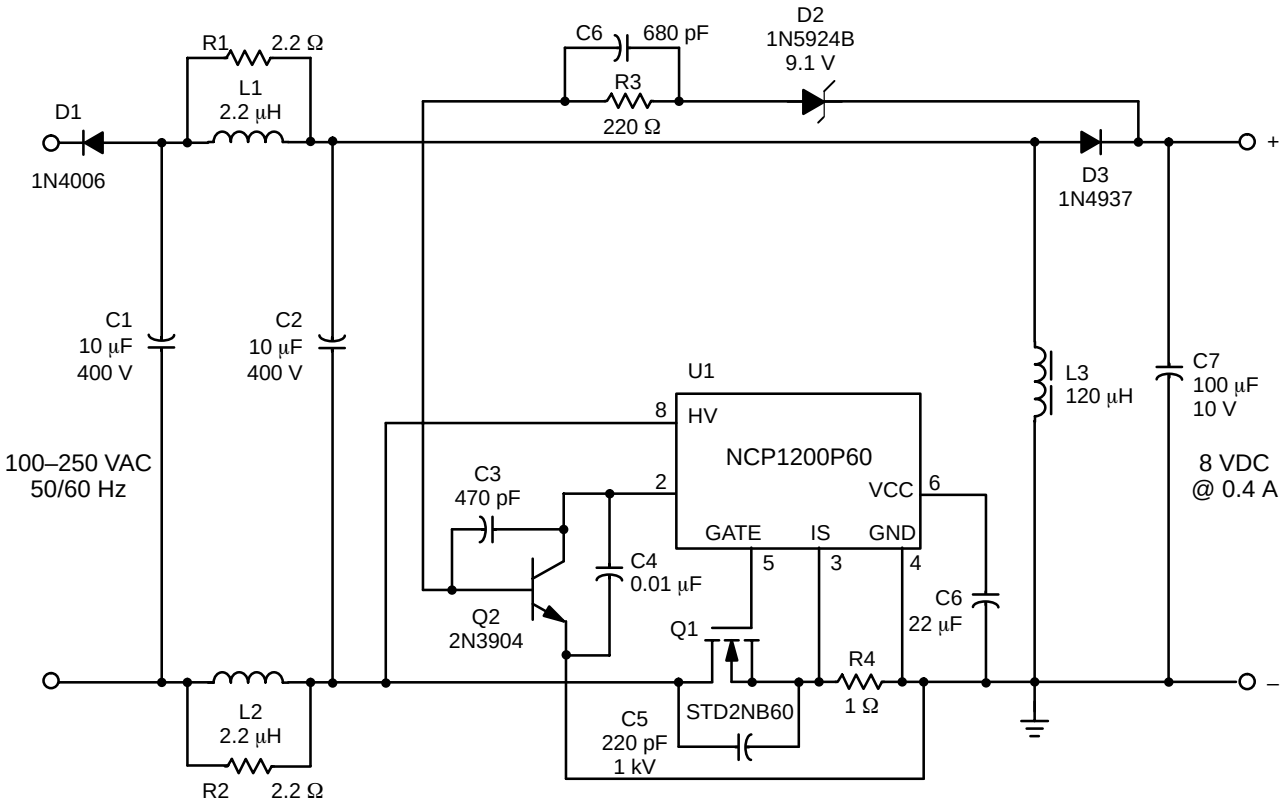

Figure 1. Non–Isolated Universal Input Buck–Boost Converter Employing the 60 kHz–NCP1200

January, 2002 – Rev. 0
Publication Order Number:
AND8078/D

NCP1200

At the heart of the converter is the NCP1200 off–line current–mode PWM converter IC. This controller features a Dynamic Self–Supply (DSS) that allows it to be powered directly from the high voltage rectified line voltage. This IC also features a current–mode controller with skip cycle capability, an internally set fixed frequency oscillator (available in 40 kHz, 60 kHz and 100 kHz), extremely low no–load standby power, and built–in frequency jittering for reduced EMI.

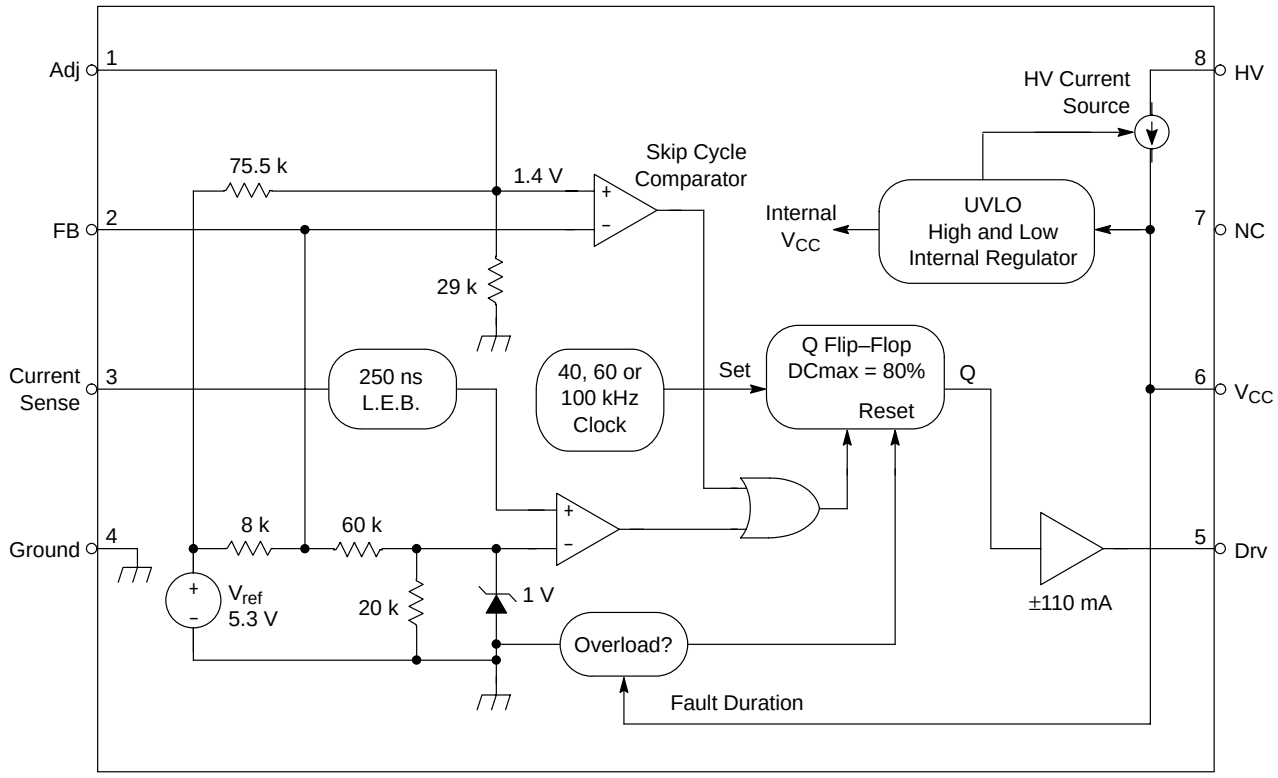

Figure 2. NCP1200 – Internal Circuit Architecture

Buck–Boost Topology

The basic Buck–Boost topology, shown below in Figure 3, is typically attributed as an inverting circuit since the output has the reverse polarity of the input voltage. More commonly the isolated version of this converter (Flyback) is used.

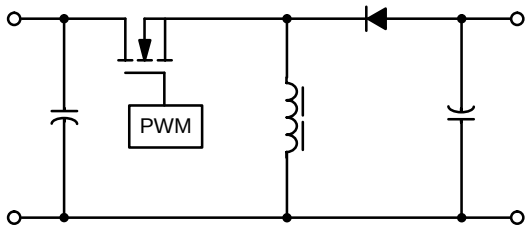

Figure 3. Buck–Boost Topology

The magnetic element in the Flyback converter simply replaces the inductor in Figure 3 with a coupled inductor with two or more winding and repositions the switch to the low side to facilitate gate drive, which reveals the more common off–line circuit topology.

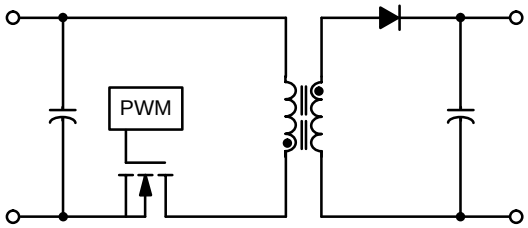

Figure 4. Flyback Converter

The converter shown in Figure 1 is essentially the same topology as Figure 3 except that the switching device has been placed on the bottom rail and the polarity of the input and output voltage has been reversed to produce a positive output voltage from a negative input source.

Derivation of the Output Characteristic Equation

This converter was designed to operate in discontinuous conduction mode (DCM). As with all switched–mode converter topologies the characteristics equation relating the input to output voltage made be derived from a fundamental analysis of the topological modes of the converter. The modes of the converter are examined by redrawing the circuit for each of the distinct cases of conduction of the active and passive switches.

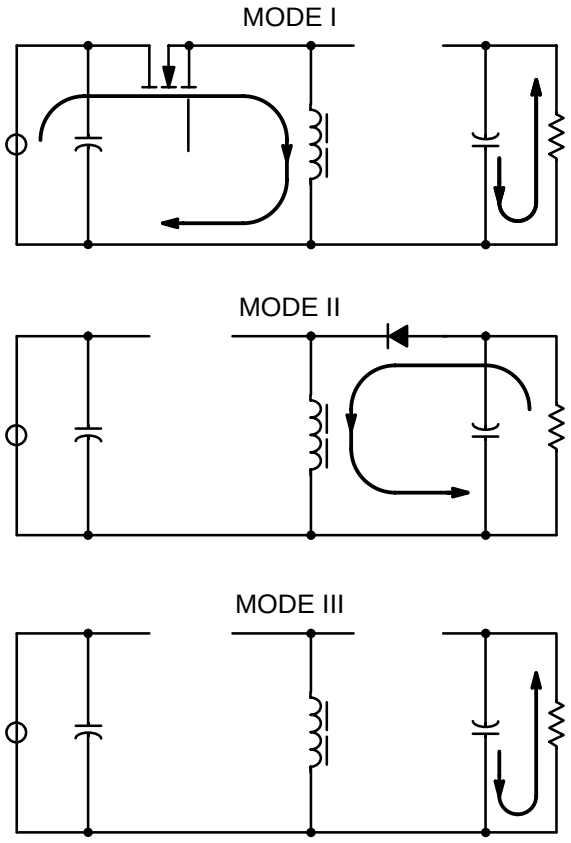

Figure 5. Topological Modes of the Buck–Boost Converter in DCM

In DCM, there are three distinct operating modes. In mode I, the switch is "on" and the input source is connected to the inductor, the output load is supported by the output capacitor since the rectifier in this case is reverse–biased. During mode II, the main switch (Q1) is turned off and the inductor voltage acts as a source polarity switch and reverses it voltage. This in turns causes D1 to conduct and the load current is supported by the stored energy in the inductor. In the third mode, neither the switch nor diode is conducting since the inductor current has fallen to zero. In equilibrium the volt–time product across the inductor during the first two modes must be equal (shaded regions on Figure 6), this information can be used to derive the input–output voltage characteristic equation that is valid for both continuous and discontinuous conduction–mode.

$$-\,Vin \cdot t_{on} = Vo \cdot t_{off} \tag{1}$$

$$\frac{Vo}{Vin} = -\frac{t_{on}}{t_{off}} \tag{2}$$

Idealized converter waveforms for the all the pertinent active and passive devices are shown in Figure 6. The average diode current (I_D) is the output load current (Io); an expression for the output current may be derived as:

$$Io = \frac{t_{off} \cdot Ipk}{2 \cdot Ts} \tag{3}$$

Where *Ts* is the switching period, and *Ipk* is given as:

$$Ipk = \frac{Vin}{L} \cdot t_{on} \tag{4}$$

Combining terms and rearranging equation (3) and (4), we can solve the "off–time" as a function of input voltage (*Vin*), switch "on–time" (t_{on}), switching period (*Ts*), inductance (*L*) and load current (*Io*).

$$t_{off} = \frac{2 \cdot Ts \cdot L \cdot Io}{Vin \cdot t_{on}} \tag{5}$$

The "off–time" can also be expressed as a function of the switching period (*Ts*), inductance (*L*) and load resistance (*Ro*). Simply substitute *Ipk* from equation (4) into the equation for *Io*; equation (3), which yields:

$$Io = Vin \cdot \frac{t_{on} \cdot t_{off}}{2 \cdot Ts \cdot L} \tag{6}$$

Solving for |*Vin*| in equation (2) and substituting it into (6) yields:

$$Io = Vo \cdot t_{off}^{\,2} \cdot \frac{1}{2 \cdot Ts \cdot L} \tag{7}$$

Rearranging (7) and substituting *Ro* for *Vo/Io*, we find that the "off–time" may be expressed as:

$$t_{off} = \sqrt{\frac{2 \cdot Ts \cdot L}{Ro}} \tag{8}$$

Another essential parameter of this converter is the duty cycle (α_D), which is the ratio of "on–time" to the switching period (t_{on}/Ts). The equation for the duty cycle is by solving for the "on–time" in equation (2), and substituting the result of t_{off} from equation (5):

$$\alpha_D = \frac{1}{Vin} \cdot \sqrt{\frac{2 \cdot Vo \cdot Io \cdot L}{Ts}} \tag{9}$$

Since, $\alpha = t_{on} / Ts$ and $(1–\alpha)$ is t_{off} / Ts, the expression for the duty–cycle (α_C) of a buck–boost converter is continuous conduction mode (CCM) is load independent and may be derived from (2) as:

$$\alpha_C = \frac{Vo}{Vin + Vo} \tag{10}$$

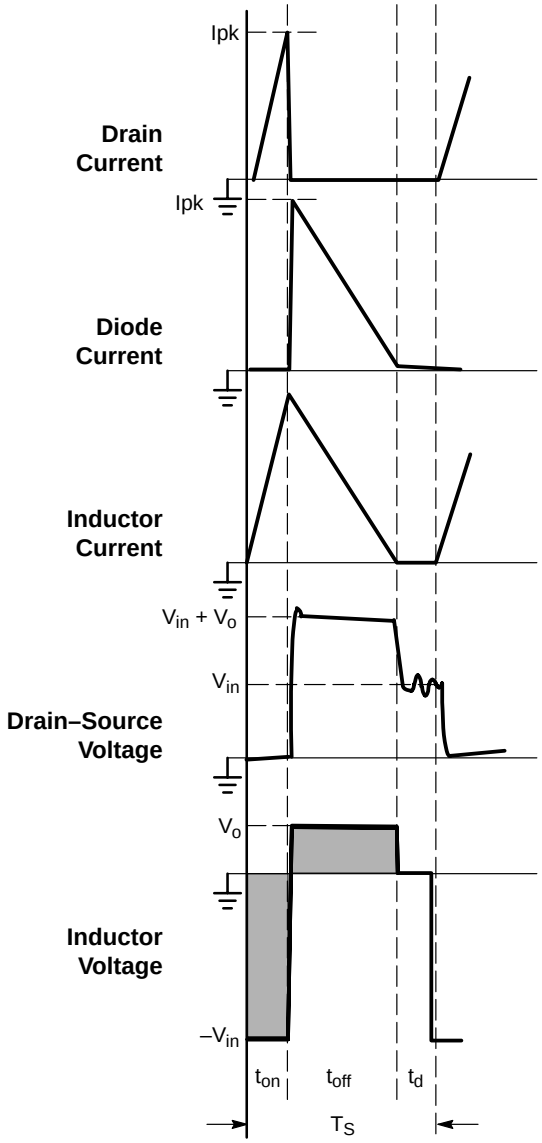

Figure 6. Idealized Converter Waveforms

Input Stage Design

A half–wave rectified input stage was selected to reduce cost and overall part count. This basic circuit comprises of a standard recovery rectifier and single high voltage capacitor. The only constraint of this circuit is peak–to–peak voltage ripple on the bulk capacitor and its affect on the output. A smaller bulk capacitor will allow higher 120 Hz ripple on the DC bulk voltage and depending on the loop dynamics a higher amount of this frequency component on the output voltage. Using the technique outlined in [1], we find that a total bulk capacitance of 20 μF will suffice for this circuit. Please note that a capacitor of with roughly half of this capacitance would have been required had we opted to use a full bridge rectifier. Figure 7 shows the PSPICE simulation results for the bulk capacitor voltage with a half–wave rectified input source at 100 VAC/60 Hz into the input filter arrangement shown in Figure 1 with a constant 4.7 W load (assumes 75% efficiency).

The following chart tabulates the results of this simulation for high and low line conditions maximum rated load.

Table 1. Input Filter Simulation Summary

Vin	100 VAC/60 Hz	250 VAC/50 Hz
Vmin	78.3 V	339 V
Vmax	112.8 V	352.2 V
$Vavg_{DC}$	96.4 V	344.7 V

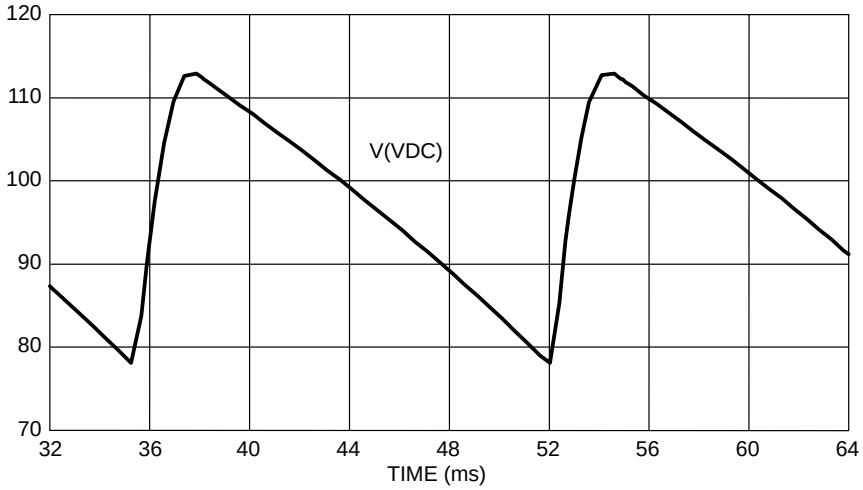

Figure 7. Simulation Plot of the Bulk DC Capacitor at Low Line

DC Analysis

The expected duty cycle of the converter can be computed over the operating line range using the expressions we derived above. The converter can be expected to operate over a relatively broad range of duty–cycles, which span the expected line and load range. At no–load and light load conditions, the NCP1200 will enter into a skip–cycle mode whereby the input power and peak current limit will be significantly reduced. The inductor value was chosen to maintain DCM operation for all operating conditions. An expression for the critical inductance (inductance value at the border between CCM and DCM) may be derived from solving for L in equation 8:

$$Lc = \frac{Vo}{Io} \cdot (1 - \alpha)^2 \cdot Ts \qquad (11)$$

Solving the critical inductance equation above for low line conditions (Vin = 96.4 VDC) and our load current and output voltage, we find that the desired inductance to remain in DCM must be less than 142 μH. Using this inductance will cause the converter to operate at critical conduction–mode; the operating duty cycle (α) at low line is 7.7% (t_{on} = 1.28 μsec). The design value of the inductor in this example was chosen to be 120 μH. We can also find that the peak switch and inductor current will stay relatively constant over the line range at our rated load. The peak switch current using an inductance of 120 μH (not accounting for circuit losses) is 0.94 A.

Current Sense Resistor

Again using the guidelines from [1], we find that a suitable value for the sense resistor is 1.0 Ω. The peak switch current limit neglecting the propagation delay of the NCP1200 will be approximately 0.9 V/1.0 Ω = 0.9 A. This value is confirmed in the simulation results and breadboard example of the circuit, which are discussed in subsequent sections.

Device Selection

The only design constraints for the MOSFET are its drain–source voltage and drain current ratings. For this design, the minimum VDS rating is Vin_{MAX} + *Vo = 353 + 8 = 361 V,* and minimum drain current rating of ~1.0 Apk. The breadboard example utilizes a ST–Micro STD2NB60E, which has a VDS rating of 600 V, ID = 2.2 A with an rDSon of 3.6 Ω. The output rectifier must be rated to handle the average output load current of 0.4 A, a peak current of 0.9 A, and a breakdown voltage of 293 V. A low cost leaded ultrafast rectifier (1N4937) was chosen, which is rated at 600 V/1.0 A.

Output Voltage Regulation

The output voltage of this converter is regulated using a zener diode and NPN transistor. The output voltage is the zener voltage + the Vbe voltage–drop of the transistor. A more precise output voltage can be achieved using a TL431, which will also allow traditional loop compensation techniques. Figure 8 depicts a possible implementation of the TL431 shunt regulator for precise output voltage regulation.

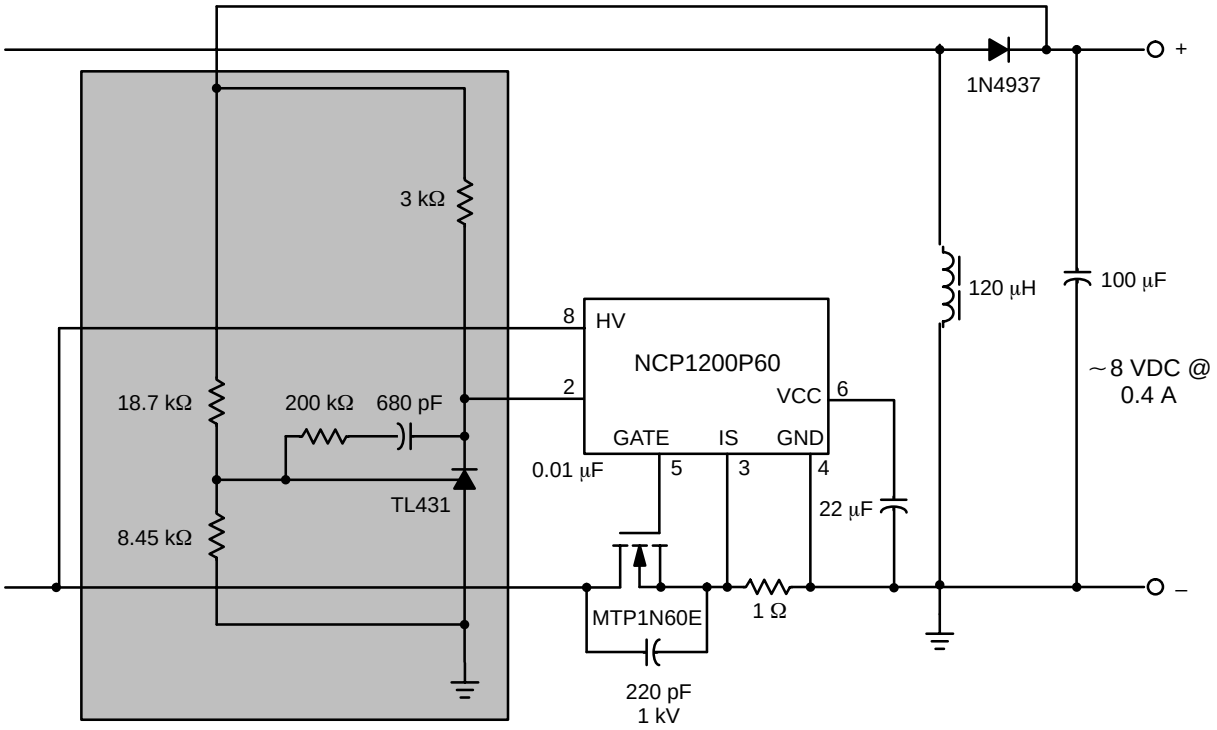

Figure 8. TL431 Implementation for Precise Output Voltage Regulation

Compensating the zener regulator can be achieved by adding an RC network from collector to base of the transistor and/or adding a parallel capacitor to the resistor which is between the zener and transistor base. This resistor not only sets the bias conditions for the transistor and zener, but also sets the open–loop gain of the circuit. The additional capacitor across the base–collector of the transistor will help roll off its inherent high frequency gain and more importantly the converter.

Simulation Results

The following plots are results of a transient simulation performed on PSPICE. The simulation schematic is shown in Figure 9, followed by plots of the output voltage, drain–source voltage, current sense resistor voltage and inductor current.

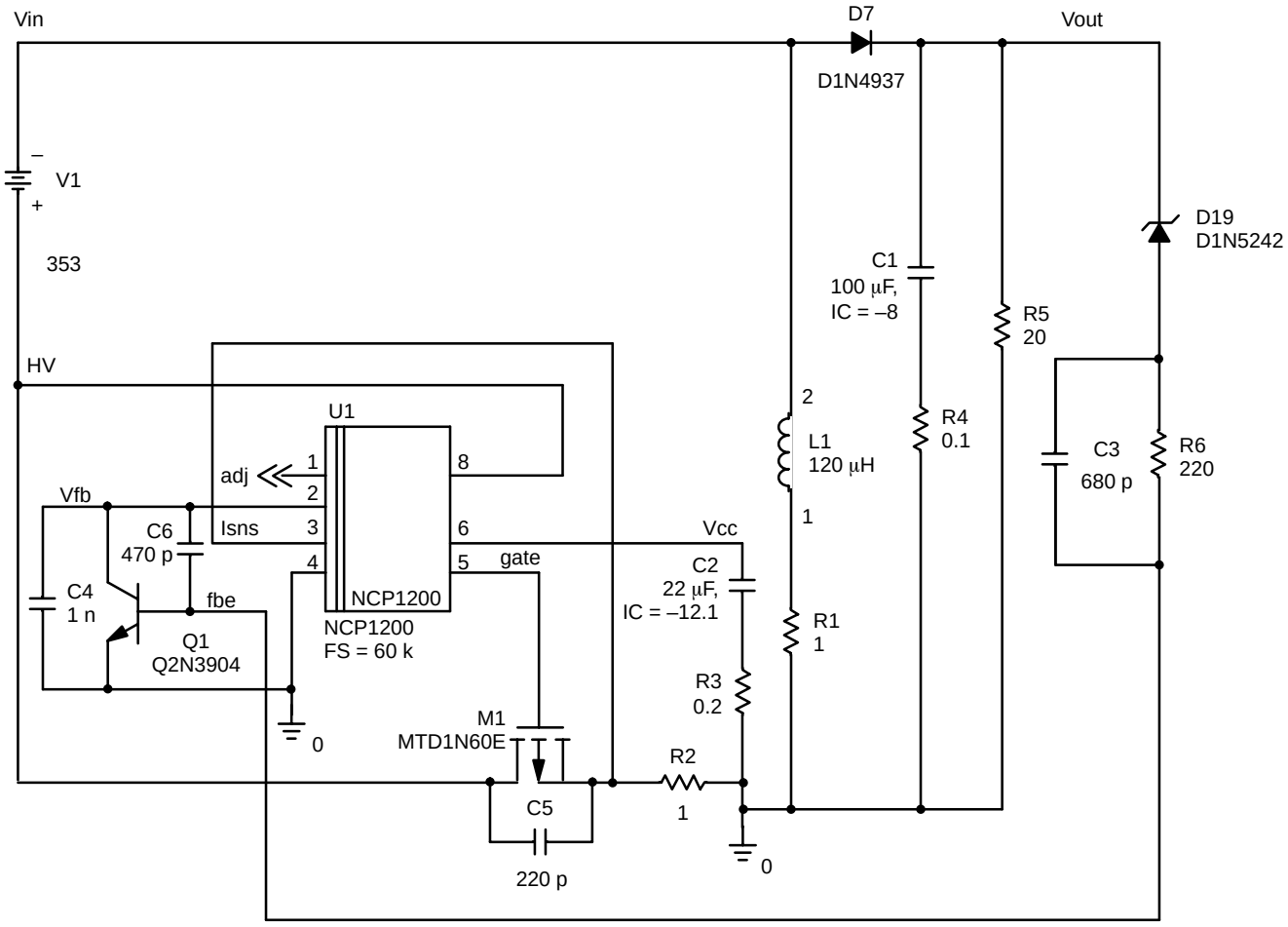

Figure 9. PSPICE Simulation Schematic

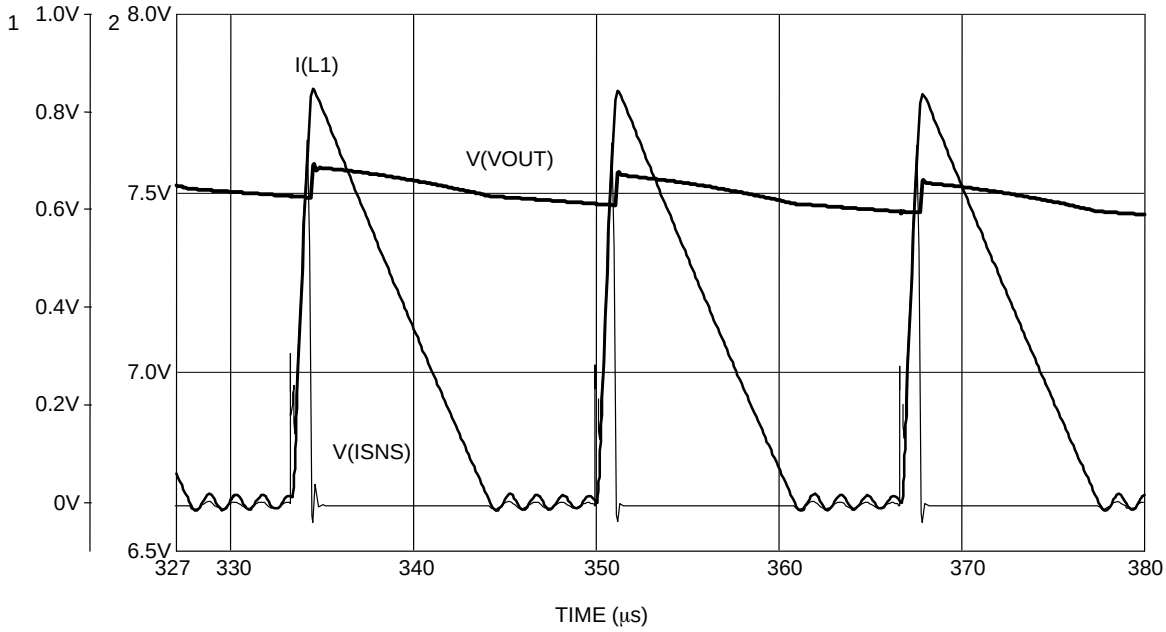

Figure 10. Simulation Results – Output Voltage, Current Sense Voltage, and Inductor Current
Vin = 96.4 VDC, Ro – 20 Ω

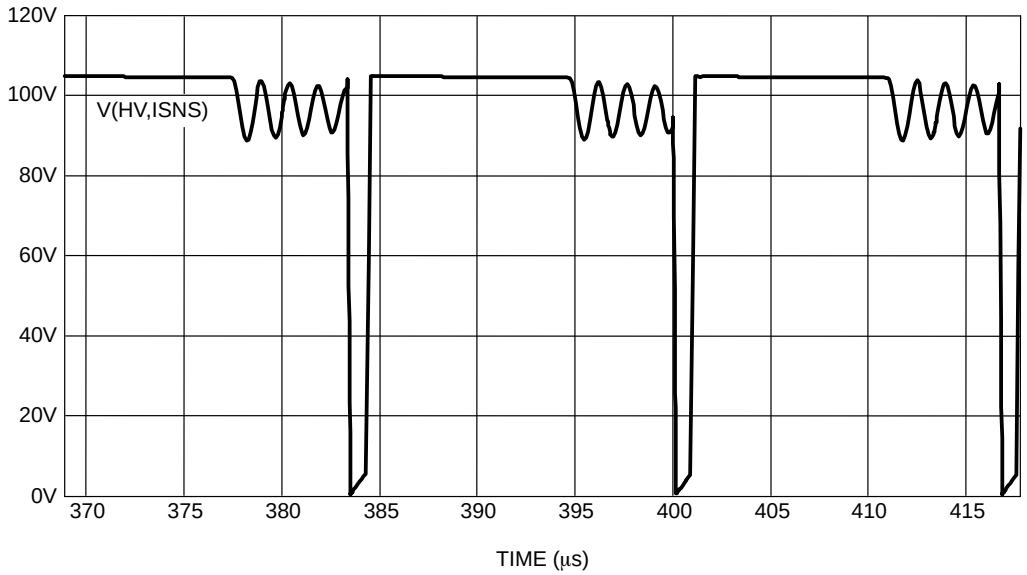

Figure 11. Simulation Results – MOSFET Drain–Source Voltage
Vin = 96.4 VDC, Ro – 20 Ω

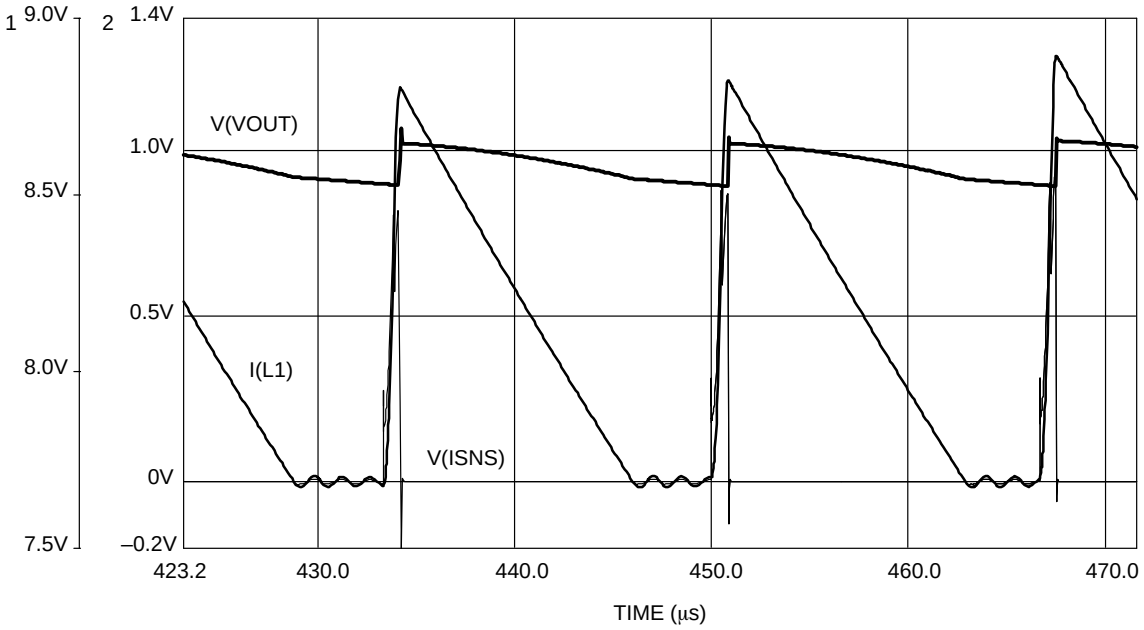

Figure 12. Simulation Results – Output Voltage, Current Sense Voltage, and Inductor Current
Vin = 353 VDC, Ro – 20 Ω

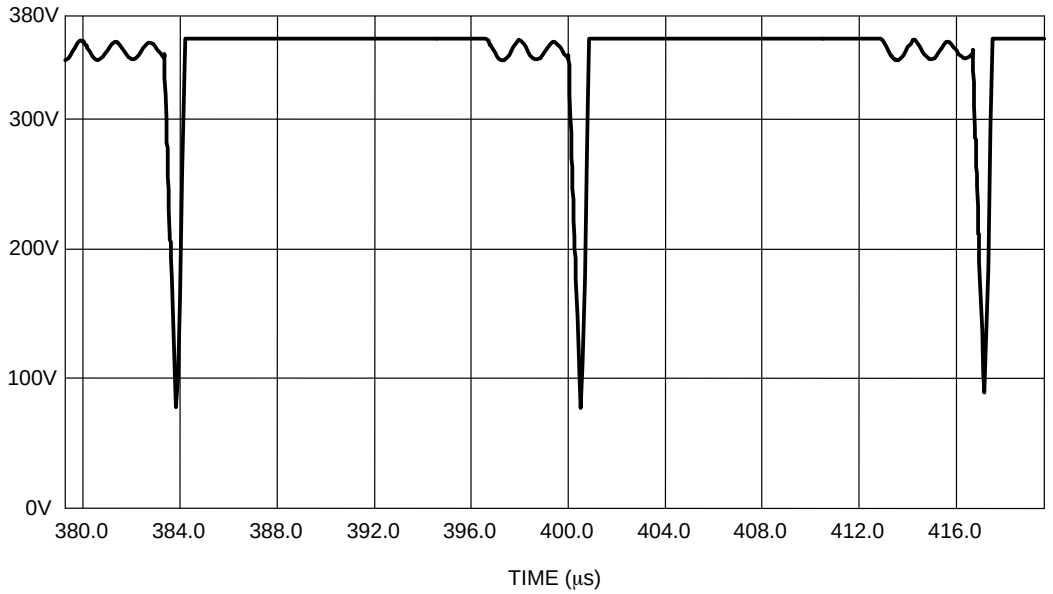

Figure 13. Simulation Results – MOSFET Drain–Source Voltage
Vin = 353 VDC, Ro – 20 Ω

Actual Hardware Oscillographs and Performance Summary

The circuit shown in Figure 1 was built to validate the analysis and verify operating specifications. The following plots show the output voltage at full load and no–load, as well as the drain–source voltage, current sense resistor voltage, and bulk DC voltage at full load. A figure showing regulation voltage over the line and load range is shown in Figure 18.

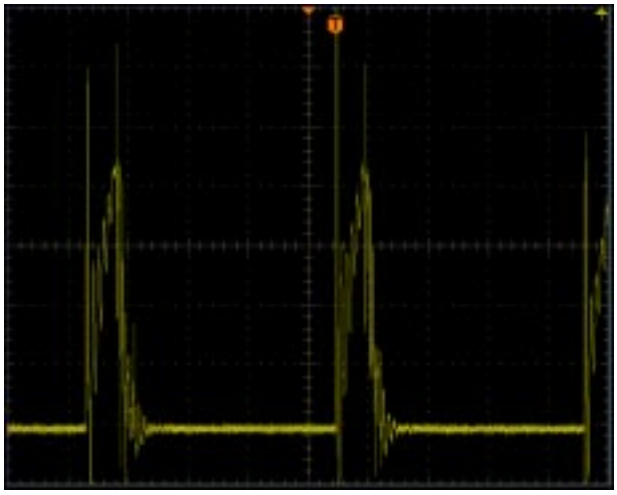

Figure 14. Hardware Oscillograph – Current Sense Resistor Voltage
Vin = 100 VAC/60 Hz, Ro – 20 Ω

Figure 15. Hardware Oscillograph – VD Voltage Waveform
Vin = 100 VAC/60 Hz, Ro – 20 Ω

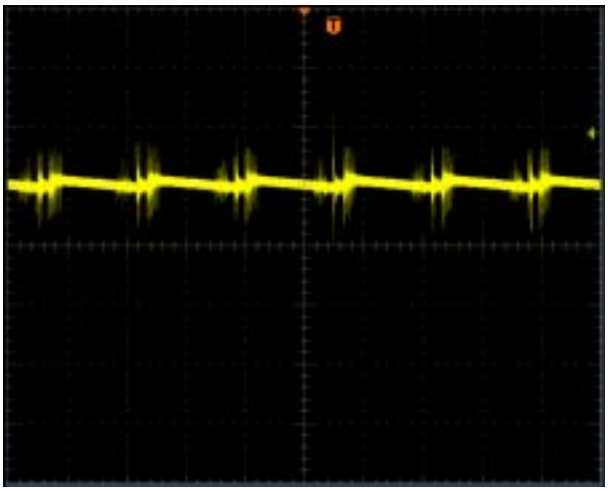

Figure 16. Hardware Oscillograph – Output Voltage
Vin = 100 VAC/60 Hz, Ro – 20 Ω

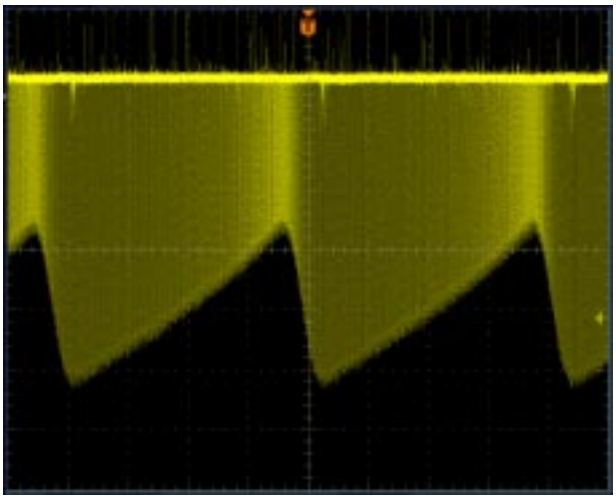

Figure 17. Hardware Oscillograph – Bulk DC Voltage with Respect to Circuit GND
Vin = 100 VAC/60 Hz, Ro – 20 Ω

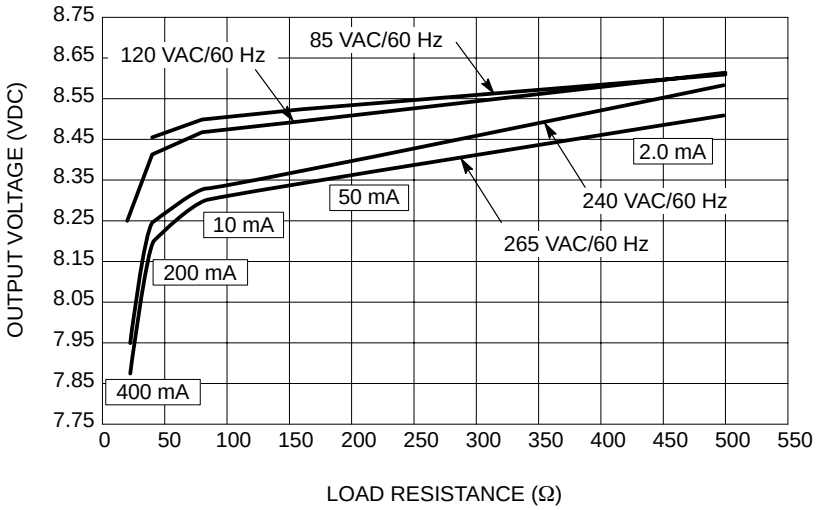

Figure 18. Hardware Operating Characteristics (Line/Load Regulation)

PCB

The complete bill of material and PCB component silkscreen and artwork layers are shown for the NCP1200 design example. The PCB is a single sided CEM1 chosen for its low manufacturing cost.

BILL OF MATERIAL

Ref Des	Part No.	Part Description	Manufacturer	Geometry
R1, R2	–	2.2 Ω, 1/4 W Metal Film Leaded	–	Axial
R3	–	220 Ω, 1/8 W Metal Film Leaded	–	Axial
R4	–	1.0 Ω, 1/2 W	–	Axial
C1, C2	URS2G100MHA	10 μF, 400 V, Alum. Electrolytic	Nichicon	16 x 15 mm
C3	–	470 pF, 50 V, Monolithic Ceramic Disc	–	–
C4	–	0.01 μF, 50 V, Monolithic Ceramic Disc	–	–
C5	–	220 pF, 1.0 kV, Monolithic Ceramic Disc	–	–
C6	UHC1C220MDR	22 μF, 16 V, Alum. Electrolytic	Nichicon	5 x 7 mm
C7	UHC1C101MDR	100 μF, 16 V, Alum. Electrolytic	Nichicon	6.3 x 11 mm
L1, L2	9130–28	2.2 μH, 395 mA, RDC = 0.4 Ω, Axial Leaded Molded RF Choke	JW Miller Magnetics www.jwmiller.com	Axial
L3	–	120 μH, 1.5 A	–	–
D1	1N4006	Standard Recovery 800 V, 1.0 A	On Semiconductor	Case 59–03
D2	1N5924B	Zener Voltage Regulator, 9.1 V, 3.0 W	On Semiconductor	Case 59–04
D3	1N4937	Fast Recovery Diode, 600 V, 1.0 A	On Semiconductor	Case 59–03
Q1	STD2NB60	N–Channel MOSFET, 600 V/3.6 Ω	STMicroelectronics	I–PAK
Q2	2N3904A	General Purpose, NPN, 30 V/100 mA	On Semiconductor	TO–92
U1	NCP1200	Off–Line Current Mode PWM Controller IC	On Semiconductor	DIP–8

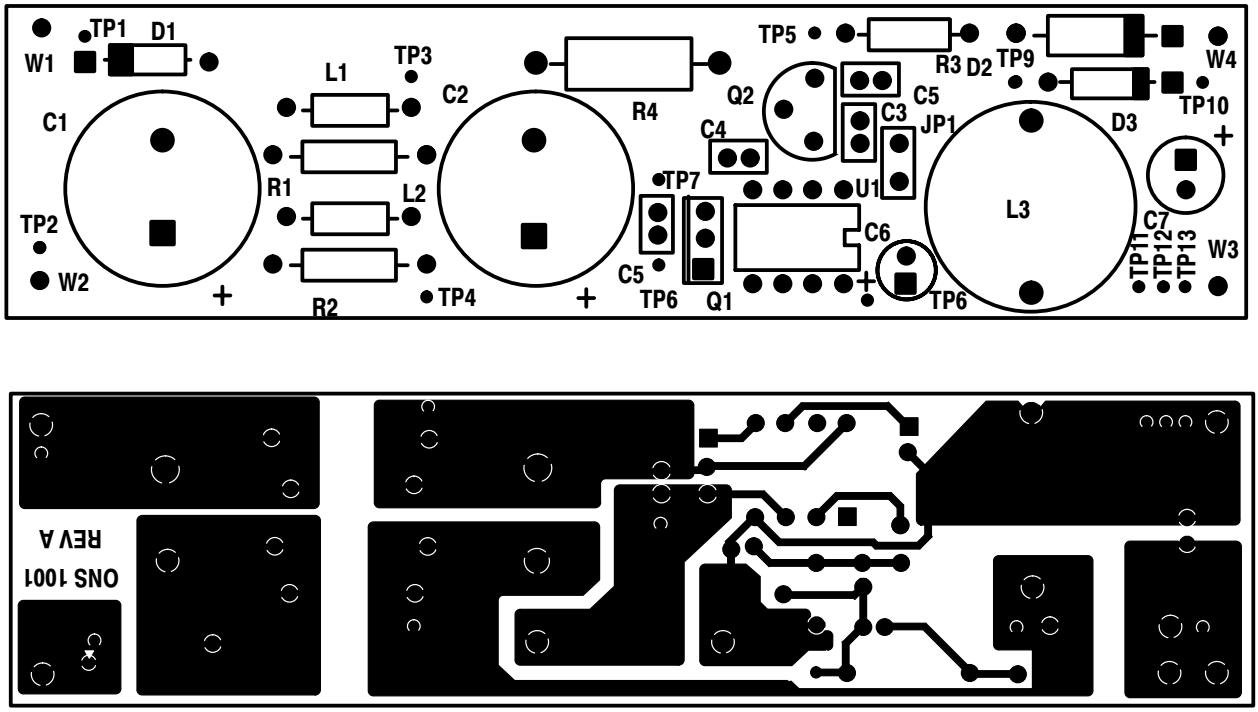

Figure 19. PCB Silkscreen and Artwork

Alternate Embodiment

The circuit shown in Figure 1 is a non–isolated off–line converter with a key deficiency is some applications, in the fact that both the line (hot) and neutral AC inputs are switched. The MOSFET drain (switching node) is connected to the neutral and the line (hot) is tied to a rectifier, necessary to develop the required DC voltage for conversion. This configuration has potentially serious safety issues. For safety, the circuit shown below maintains a ground referenced neutral line and which is common to the output return.

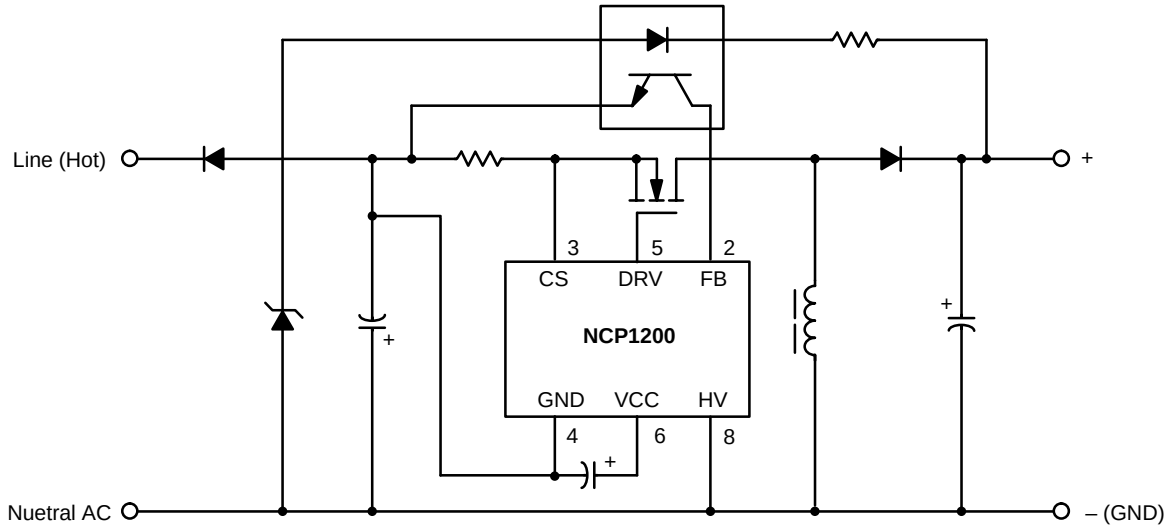

Figure 20.

In this circuit transformation, the MOSFET source is tied to the line and the neutral is at ground potential. In order to regulate the output voltage, an opto–coupler must be used in the feedback loop to overcome differences in the common–mode voltage potentials between the output and FB pin of the control IC. This is due to the fact that the NCP1200 is now referenced to the rectified AC line (hot).

Conclusion

This paper detailed the design and analysis, including device selection criteria, for a non–isolated off–line buck–boost converter. The NCP1200 series offers sufficient flexibility to configure this topology for various output voltage and power requirements. Alternatively, the NCP105x series of off–line gated–oscillator ICs may also be used in this topology.

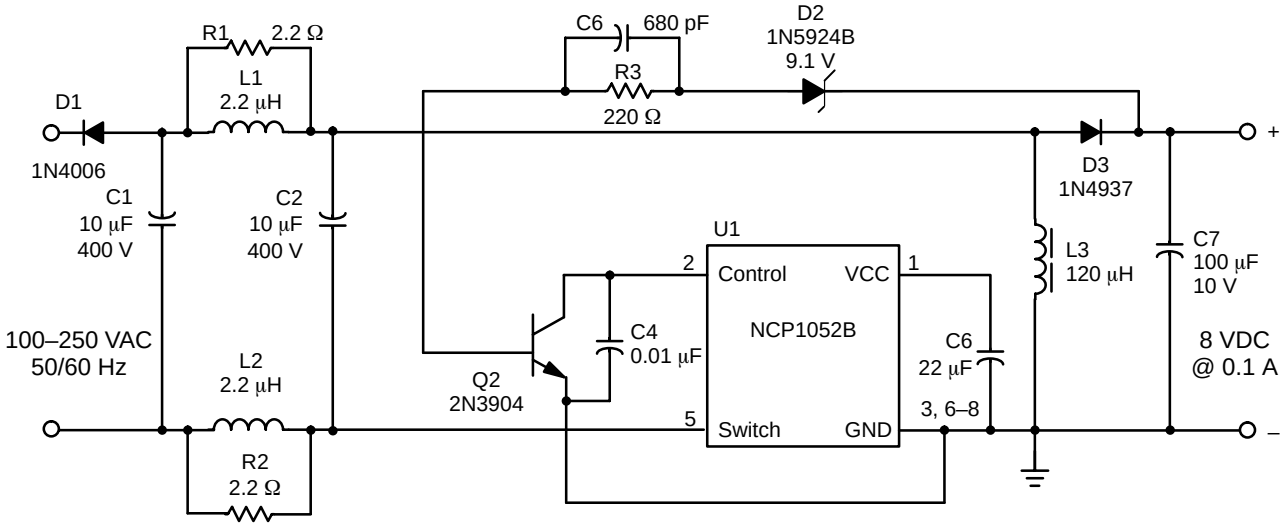

Figure 21. Adaptation with the NCP1052B

The NCP105x series feature an on–chip 700 V power switch, a unique dual–edge gated oscillator for extremely fast loop response, high voltage start–up and operation, frequency dithering for reduced EMI filtering, and an internally set frequency options (44, 100 and 136 kHz). The distinct advantage of this IC in this converter is the lower overall part count since the MOSFET and current sensing resistor are internalized. The NCP105x series and its derivatives are offered in a wide variety and combinations of switching frequency and peak current limits. In either case whether it be a NCP1200 or NCP105x, the key features and attributes of these ICs make them uniquely suitable to configure this topology for very low cost off–line power conversion.

Acknowledgments

The author would like to acknowledge Douglas K. Thomson, Sr. Design Engineer with ABB Automation Inc., in Raleigh, NC, for inspiring this application note as well as the insightful conversions relating to this topic.

References

1. AN8023/D, “Implementing the NCP1200 in Low–Cost AC/DC Converters”, Christophe Basso, October 2000.
2. AN8038/D, “Implementing the NCP1200 in a 10W AC/DC Wall Adapter”, Christophe Basso, October 2000.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.