# Intusoft Newsletter

*Personal Computer Circuit Design Tools*

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# Native Mixed Mode

On December 12, 1994 Intusoft will release a new version of ICAP/4Windows. The new version will include two new major enhancements: an expanded set of built-in SPICE models and a digital logic simulator capable of providing native mixed mode simulation. Current ICAP/4Windows owners may update to the new version for $295. For those that have bought ICAP/4Windows since October, the upgrade is free (But you must send in your free update card!!). For new customers, the price of ICAP/4Windows will not be increased. Many other vendors talk about giving the customer value; Intusoft delivers.

The main addition to the IsSpice4 program is a set of new analog,

*continued on page 2*

**In This Issue**



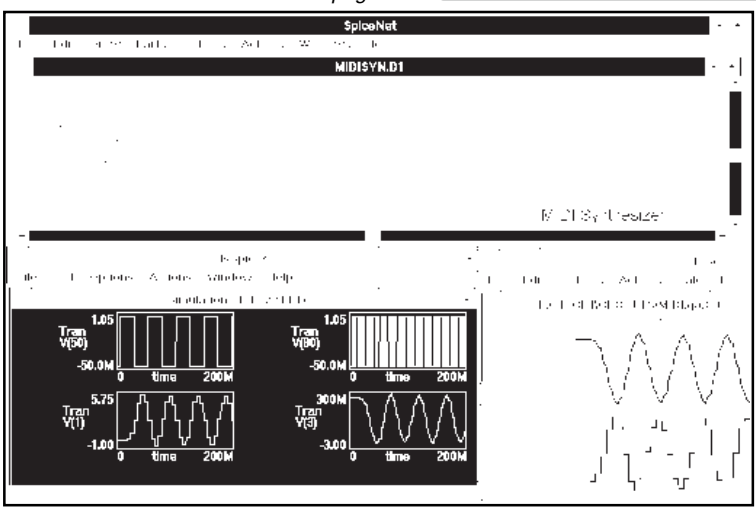



**Figure 1,** New models in the IsSpice4 program help simulate Mixed Mode problems like this MIDI synthesizer. See pg. 6 for more details.

# New IsSpice4 Has More Models

*continued from page 1*

hybrid (mixed analog/digital), and digital code models. Code models are an extension of the standard devices offered in SPICE programs and provide you with an enriched set of modeling primitives with which to build subcircuit models. The models are accessed in the same manner as SPICE primitive elements such as a diode or BJT. Some of the over 40 analog, hybrid, and digital primitives are shown in Table 1.

Also included is an event driven logic simulator, inside IsSpice4, providing a powerful NATIVE mixed mode simulation capability. All the new digital models allow accurate specification of propagation and rise/fall time delays.

Other IsSpice4 enhancements include:

- Arbitrary phase delay on ALL independent sources

  V1 1 0 Pulse 0 1 0 1U 1U 20U 40U 45 ; 45 causes the output of V1 (node 1) to start with a 45 degree phase shift at time 0. This contrasts the TD (delay time) parameter which simply delays a zero phase version of the signal until the delay time has elapsed.

- User defined supply ramping to mimic actual board level turn on behavior

  .OPTIONS RAMPTIME=10N ; This would cause all independent sources in the circuit to linearly ramp up over a 10ns interval at the start of the simulation. This allows realistic modeling of circuit turn-on behavior.

- Several convergence enhancements have been added. For example, an optional user defined resistance to ground from every node to alleviate convergence

| **Analog Code Models** | **Digital Code Models** |
|---|---|
| Laplace Equations | Logic gates (Nand, Or, etc...) |
| Table Models | Flip-flops (S-R, T, D, J-K) |
| Nonlinear Magnetic Core | Frequency divider |
| System Elements: | State Machine |
| Limiters, Integrators, Slew rate, | Pull-up/down, Tristate |
| Hysteresis, Integrator/Differentiator | Latches: D, S-R |
| Analog Controlled Oscillators: | Digitally Controlled Oscillator |
| Sine, Square, & Triangle Waves | RAM |
| Controlled One Shot | |

**Table 1,** The new IsSpice4 program offers a host of new built-in models, doubling the number previously available.

problems like “No DC Path to Ground” or “Singular Matrix” conditions.

.OPTIONS RSHUNT=1E12 ; This will add a resistor of 1E12ý to ground from every node.

The upgrade also includes a new version of the SpiceNet schematic entry program and over 1000 new SPICE models bringing the total to over 6000!! These features complement the already powerful interactive operation of IsSpice4 to create a SPICE program unmatched by any other CAE tool vendor.

## Simulating A Speed-Control Servo

One of the most versatile new code models is the Laplace function block. The Laplace code model offers the designer great flexibility especially when designing feedback control systems. The diagram in Figure 2 describes the control loop of a constant cutting speed servo for a vertical boring machine. Servo control loops pose a variety of design challenges. Varying dynamic performance of different elements, such as the load, require a flexible design that allows for gain and compensation adjustments. IsSpice4 is ideal for helping you make these design decisions. The actual design consists of two control loops, one to control the position of the cutting tool and one to control the speed. In this example we examine only the speed loop. More information is available in [1].

The Laplace code model takes in numerator and denominator polynomial coefficients. For example, a 3kHz Chebyshev LP filter (=> $1/s^2 + 1.42s + 1.52$) would be written as:

**.Model Cheby_LP_3KHz S_Xfer (In_Offset=0 Gain=1**
**+ Num_Coeff=[1] Den_Coeff=[1 1.42562 1.5162] Int_Ic=[0 0 0])**

The Laplace coefficients for each block in Figure 2 were entered directly into the SpiceNet schematic through a simple dialog. SpiceNet takes care of building the Laplace .Model

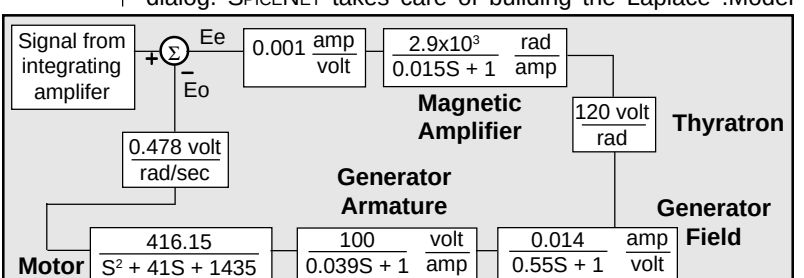



**Figure 2,** The block diagram for a speed control system.

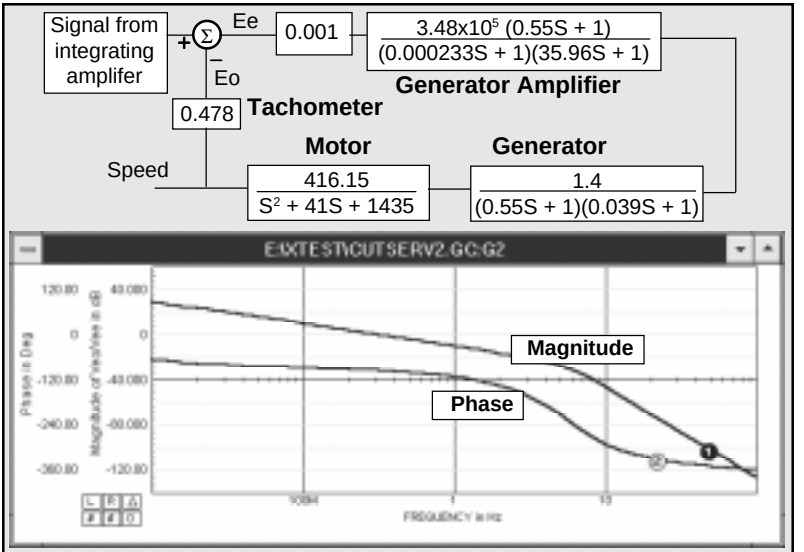
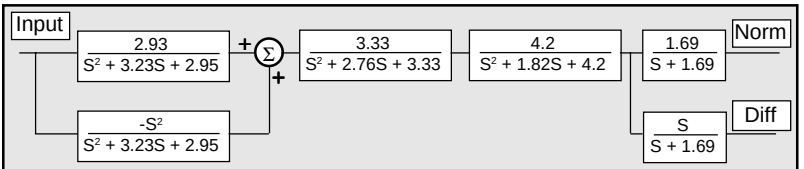



**Figure 3,** Block diagram of the compensated speed control loop. The magnitude and phase of Eo/Ee are shown.

statements. If coefficients are changed, SPICENET will update the netlist as required. Previously entered blocks can be called up and easily reused. Investigation of the initial loop design in Figure 2 showed some instabilities. A damping network was added around the amplifier to produce the system in Figure 3. With the new compensation added the loop showed good stability with a phase margin of 83 deg. and a gain margin of over 20dB.

## Simulating Filters Functions

The new Laplace code model can also be used to simulate a variety of filters. Most common filter types and approximation can easily be simulated with the straightforward entry of the proper coefficients. Instead of showing something simple, lets jump right in and try a more advanced scenario. Figure 4 shows the normalized block diagram of the SSI 32F8011




```
A2 1 2 S_001 ; Model for the top left Laplace block
.MODEL S_001 S_xfer(In_Offset=0.0 Gain=1.0 Num_Coeff=[2.94933]
+ Den_Coeff=[1.0 3.22597 2.94933] Int_Ic=[0 0 0] Denorm_Freq=94.248Meg )
```

**Figure 4,** Laplace block diagram for the SSI 32F8011 Programmable Electronic filter. An example Laplace model statement for the top left block is shown.

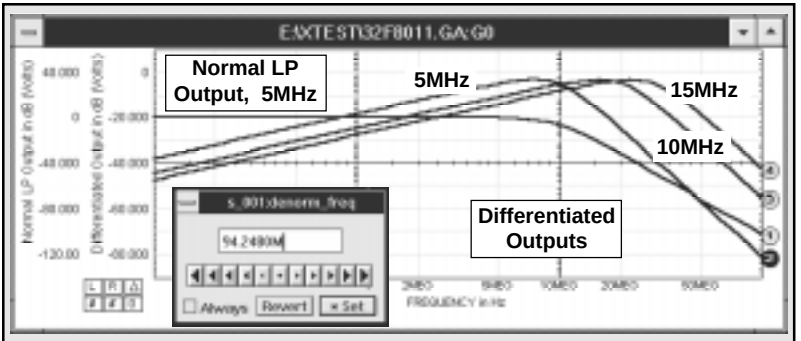



**Figure 5,** The interactive sweeping feature of IsSpice4 is used to sweep the denormalized frequency while examining the filter output.

programmable electronic filter from Silicon Systems. The IC provides a controlled low-pass filter with a separate differentiated low-pass output. The .Model statement for one of the blocks is shown in Figure 4. Figure 5 shows the normal and differentiated outputs from an AC analysis.

The model parameters can easily be reconfigured in the schematic or interactively swept in the IsSpice4 simulator. The denormalization frequency, a model parameter (Denorm_Freq), is swept in Figure 5 and 6 to measure the filter performance at 5, 10, and 15MHz. Figure 6 shows the group delay calculated by the IntuScope post processing program. Laplace models can be used in both AC and transient analyses.

The preceding examples reveal the flexibility and efficiency of the Laplace code model for electrical and non-electrical applications. Other code models provide similar benefits.

[1] George Thaler and Robert Brown, “Analysis and Design of Feedback Control Systems”, 2nd, McGraw-Hill, 1960

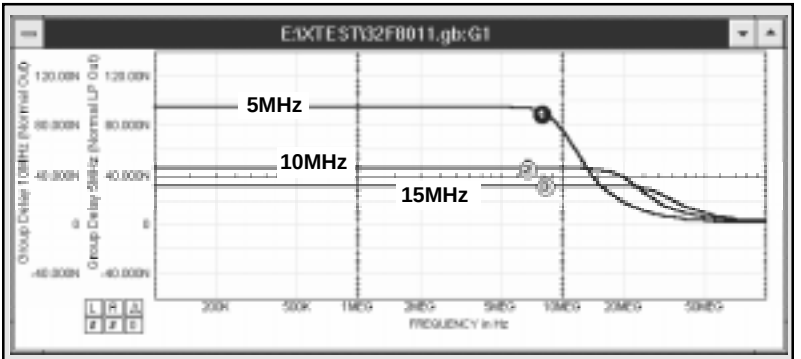



**Figure 6,** The IntuScope data analysis program can compute the group delay at any point in the circuit. The differentiated delay at 5, 10, and 15MHz is shown above.

# Native Mixed Mode Simulation

Modern circuits often contain a mix of analog and digital circuits. To simulate these circuits efficiently a combination of analog and digital simulation techniques is required. With the release of the new IsSpice4 version in December, Intusoft supports three ways to model mixed mode circuits.

- Exact transistor representations
- Boolean Logic Expressions
- Digital Primitives *plus* Embedded Logic Simulator

Exact representations are used mainly in the analysis of transmission line and signal integrity problems where a close inspection of an IC's I/O characteristics is needed. Boolean logic expressions are delayless functions that are used to provide efficient logic signal processing in an analog environment. These two modeling techniques use SPICE to solve a problem while the third method, digital primitives, use IsSpice4's new native mixed mode capability.

Digital circuit simulation differs from analog circuit simulation in several respects, but the primary difference is that a solution of Kirchoff's laws is not required. Instead, the simulator only determines whether a change in the logic state of a node has occurred and then, propagates this change to connected elements. Such a change is called an "event". When an event occurs, the simulator examines only those circuit elements that are affected by the event. By comparison, analog simulators iteratively solve for the behavior of the entire circuit because of the forward and reverse transmission properties of analog components. This difference results in a considerable computational advantage for digital circuit simulators, which is reflected in the significantly greater speed of digital simulations. Therefore, it is vastly more efficient to simulate the digital portions of a design with a digital simulator and the analog sections with SPICE. Only in cases where the two are inextricably dependent should a mixed approach be undertaken.

Two basic methods of implementing mixed-mode simulation are the "native mode" and "glued mode" approaches. Native mode simulators implement both analog and digital algorithms in the same executable and use one input netlist. Unlike SPICE 3, which is designed mainly for analog simulation, and based exclusively on matrix solution techniques, the new IsSpice4 program includes BOTH analog and event-driven digital simulation capabilities in the same executable. Thus, designs that contain significant portions of digital circuitry can be efficiently

simulated together with the analog components. Support is also included for non-digital nodes that are simulated by the event-driven algorithm. Such a node might have real values but change only at discrete time intervals. Because the event-driven algorithm is faster than the standard SPICE matrix solution algorithm, reduced simulation time for circuits that include these models can be anticipated compared to a simulation of the same circuit using only analog models.

Glued simulators actually link two separate simulators, one analog and the other digital. This type of simulator must define an input/output protocol so the two executables can communicate with each other effectively. The communication constraints tend to reduce the speed, and sometimes the accuracy, of the complete simulator. On the other hand, the glued approach allows the component models developed for the separate executables to be used without modification.

The December update provides a pre-defined collection of common analog and digital functions and provides an extensible base on which to build additional models. As a mixed mode example, we will look at the simulation of a MIDI synthesizer that utilizes analog, digital, and real valued data.

## Simulating A MIDI Synthesizer

The circuit shown in Figure 7 depicts a simple MIDI synthesizer [1]. MIDI stands for Musical Instrument Digital Interface and is used as a gateway between the analog world of music and the digital world of computers.

Simulation of the system involves three types of data; Digital, which has 12 states, real which has continuous values, and analog voltages and currents. These types are signified by the letters D, R, and A, respectively, on the schematic. Translational bridges are used to convert between signal types.

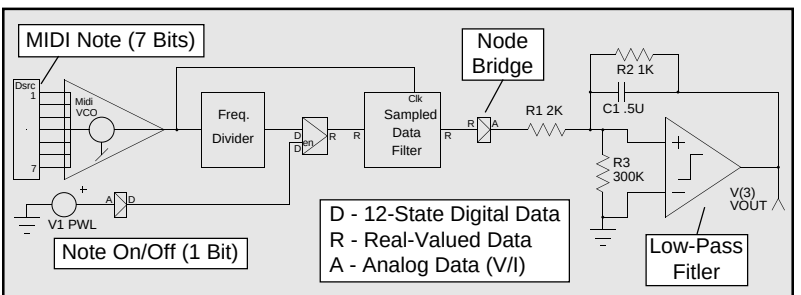



**Figure 7,** System level simulation of a MIDI synthesizer. Digital, real and analog signals, designated by the D, R, and A letters, are simulated together.

```
.Model MIDI_001 NCO (DELAY=1.0N MULT_FACTOR=16 ) ; Digitally Controlled Oscillator

.Model FDiv d_Fdiv(div_factor=8 high_cycles=4 i_count=0 rise_delay=2N fall_delay=2N)

.Model LIM2_001 Limit (Out_Lower_Limit= -12 Out_Upper_Limit=12 Fraction=True
+ Limit _Range=0.2  Gain=300K)  ; Limiter Code models

.Subckt  DIG_FILTER  Filt_In Clk Filt_Out  ; Partial Sampled Data Filter Listing
*
.MODEL N0 Real_Gain (Gain=1.0)                AN0A FILT_IN X0A N0  ; Digital Filter con't
.MODEL N1 Real_Gain (Gain=2.0)                AN1A FILT_IN X1A N1
.MODEL N2 Real_Gain (Gain=1.0)                AN2A FILT_IN X2A N2
.MODEL ZM1 Real_Delay                         AZ0A X0A CLK X1A ZM1
                                              AZ1A X1A CLK X2A ZM1
```

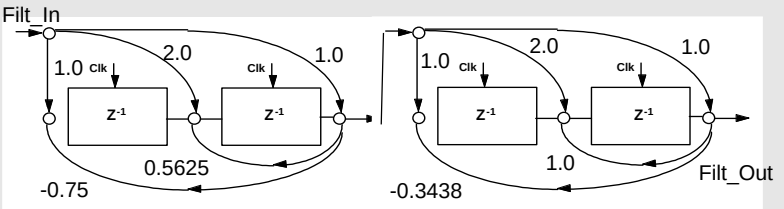



**Figure 8,** Model statements for the new numerically controlled oscillator, frequency divider, and limiter code models. A partial netlist and block diagram for the sampled data filter is shown including the models for the real and Z transform blocks. All of the new code models are available in the December release of ICAP/4Windows.

The MIDI note data is created using a digital stimulus source, Dsrc. MIDI notes, composed of 7 bits, are numbered between zero and 127 (Bit 1 = MSB). Note number zero corresponds to a C 5 octaves below middle C. There are 12 notes per octave, so a middle C (which is 261.62 Hz) is note number 60. A440 (A above middle C) is note number 69, and so forth. Three C notes were simulated, each an octave apart, corresponding to the note numbers 60, 36 and 48.

The MIDI VCO (NCO model) is a digitally controlled oscillator that produces a square wave based on the input. The frequency multiplier model parameter (see Figure 8) is 16. (Note that the sampled data filter output has 8 steps per cycle.) The frequency divider, which is also a new digital code model, uses 8 for its divide factor. The purpose here is to end up with the original note frequency. The reason we multiplied by 16 first and then divided by 8 is so we would have a 2x clk signal to drive the sampled data filter. Figure 8 shows the model statements for the NCO and Frequency divider, and a partial description of the sample data filter.

The sampled data filter uses real values and is composed of gain and $Z^{-1}$ transform code models. The input is translated from a digital state to a real value using the D-to-R node bridge. The enable on the D-to-R bridge is driven by the MIDI note on/off bit. The output is converted to an analog signal through a real-to-analog bridge and a low pass filter. The low pass filter also uses

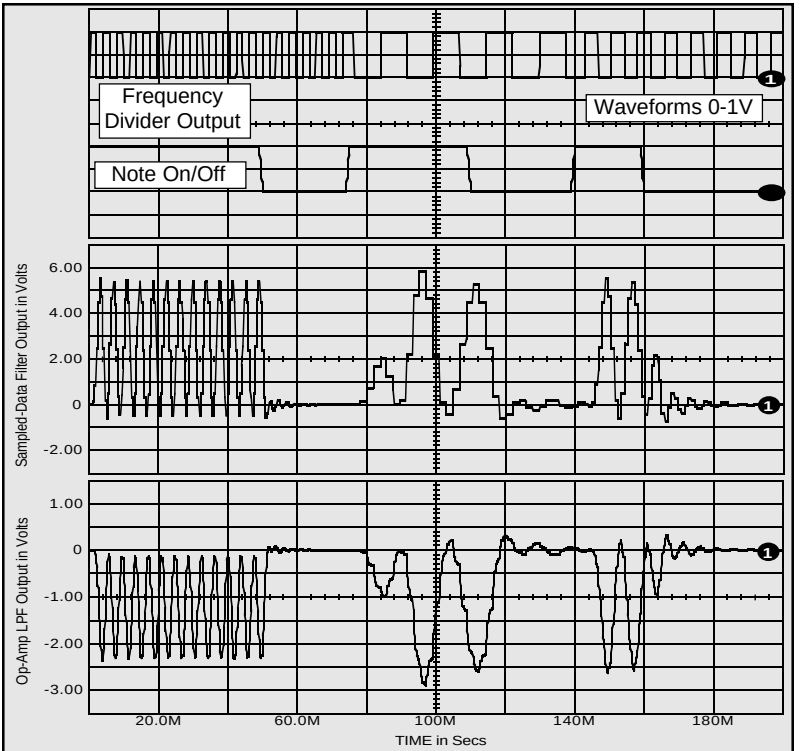



**Figure 9,** Output waveforms from the MIDI synthesizer circuit. Three frequencies were simulated over the 0.2s time span.

a limiter code model to speed the simulation. Several output waveforms are shown in Figure 9. The circuit simulates in 22.7s on a Pentium/90.

## Code Models Are The Key

The new analog and digital code models used in this simulation are available in the December release of ICAP/4Windows. In the 1st quarter of 1995, Intusoft will release a code model development kit that will allow end users to develop their own models and dynamically link them to the IsSpice4 simulator.

Code models open up many SPICE simulation boundaries allowing efficient board and system level simulations. In addition, code modeling will allow more in-depth explorations of control systems and non-electrical applications in the neural network, mechanical, hydraulic, and radiation fields.

[1] "Code-level Modeling in XSPICE", Fred. L. Cox III, William B. Kuhn, Jeffery Murray, and Stephen Tynor, Proceedings of the 1992 Intl. Symp. on C&S, San Diego, CA, 5/92, IEEE 0-7803-0593-0/92

## Notes From The Back Room

Have you noticed that over the past several years our successive releases of IsSpice have run faster? We thought you may be interested in what's going on. There are 3 factors driving the speed improvement. First, compiler technology has made significant gains in optimization, second, math libraries are improving and finally, we are steadily improving the core SPICE algorithms. With our latest release, we have increased the IsSpice4 feature set by about 20%, while reducing the executable code size and improving speed by 10 to 20% for large circuits. Compiler improvements allowed us to break even in code size and performance while increasing the simulator's capability. Tuning the internal algorithms led to significant gains for large circuits. The major change was to implement the Berkeley SPICE 3 predictor-corrector and bypass algorithms. The predictor-corrector algorithms provide improved estimates of the circuit voltages and currents, thereby reducing the number of iterations. The bypass algorithm eliminates unnecessary computation of a device when its operation is stable.

The RELTOL option sets the accuracy limit for each iteration. In the past, SPICE recomputed all circuit node voltages and branch currents for each time step. Now, some are used over if they haven't changed. There will be a tendency for all nodes to approach the RELTOL accuracy, thereby grouping the overall accuracy closer to the RELTOL specification. Simulation results will be slightly different but they will still reflect the user defined accuracy.

What's in store for next year? We will continue to push the performance envelope to give you the fastest SPICE available anywhere. Large circuits that take hundreds of seconds must have their simulation times reduced by as much as 2 orders of magnitude for truly interactive design. As we see it, silicon technology will provide speed increases of 3 to 4 times a Pentium/90 within the year, for example, with the newly introduced 275 Mhz Digital Alpha and MIPS Tyne stations. Combined with symmetric multi-processing, we see a near term increase in computing power of 10 to 20 times that of the Pentium/90. By the end of this decade, the factor of 100 speed improvement will be a reality!

To harness this power, Intusoft will release a multi-threaded version of IsSpice4 in early 1995. We believe that by performing critical parts of the simulation in parallel we will achieve nearly a 4 fold speed improvement in a quad symmetric multiprocessor environment. Using parallel processors, we will bring you unparalleled speed!

# New TI Bus Interface Models

Interest in simulating I/O signals to determine the effects of packaging and interconnects on signal integrity is on the rise. Intusoft currently includes I/O models from Motorola and Philips in our libraries. Now, Texas Instruments has released the "Advanced Bus Interface SPICE I/O Models Data Book". Included are over 125 I/O models for both 5V and 3.3V devices (ABT & LVT logic families). Both package and process model parameters for TI's BiCMOS processes are included. The process parameters (nominal, strong, and weak cases) contain Level 3 MOS models, which are used by SPICE 2G.6 simulators, and advanced BSIM (Level 4) model parameters. Both are compatible with IsSpice4. TI plans to release over 100 additional models in 1995. To use these models, the engineer first connects together the I/O device model and the package model to his signal sources and load devices. Then, either the nominal or worse case process parameter are selected. The signal characteristics can then be simulated.

The models can be obtained direct from any TI Sales Offices or authorized distributor (1-800-336-5236). Information on getting the models directly from Intusoft will be available in the next *Intusoft Newsletter*.

## Fully Functional SPICE: FREE

Intusoft has posted its ICAP/4Windows Evaluation version on both CompuServe and Internet. The software, including schematic entry, IsSpice4, a small model library, and the IntuScope waveform viewer, can be downloaded for FREE. This version is limited to circuits with 15 top-level components. (Special provisions are made for subcircuits.) Through Internet you can download the kit from:

**argesim@simserve.tuwien.ac.at**

This is the ftp server for the European Simulation News magazine. Information on the server and the magazine itself, which deals with all types of simulation (not just electrical) can also be obtained by calling +43-1 58801 5374.

CompuServe has provided Intusoft with its own section under the CAD/CAM/CAE forum. Instead of being listed under the All CAD/CAM/CAE section (library #1), Intusoft will have its own library and message sections. This provides much easier access to all of Intusoft's postings including the ICAP/4 Windows evaluation version. Type Go CADDVEN at any ! prompt to get to the CADD/CAM/CAE forum.

# The Intusoft Modeling Corner

A frequently asked question of Intusoft's technical support staff is **"Do you support the models available from vendors like Analog Devices and TI."** The answer is absolutely! Hardware vendors try to make models with syntax that will work for all SPICE programs. Unfortunately, they don't always succeed. Sometimes the netlist contains non-standard syntax extensions or syntax that won't work on SPICE 2G or SPICE 3 based programs. If you are interested in getting the latest available models you should contact Intusoft first. Intusoft usually obtains vendor models before they are released in order to test them for vendors. In addition, we add schematic symbols and combine the syntactically correct models into a single library file. While you can use the models directly from the vendors it is best to get them from Intusoft because they will be fully integrated into our ICAP/4 system and be ready to use with IsSpice.

Up to date releases of new vendor models are produced bimonthly on the *Intusoft Newsletter* floppy disk which is available on a subscription basis. Over 1200 other models are available on the Vendor Supplied Op-Amp Disk. (See pg. 19)

In this issue of The Intusoft Modeling Corner we bring you some new test stimulus sources which are easier to create because of the behavioral and code models in IsSpice4.

## Stimulating Circuits: Test Generators

The models available in the December release enhance IsSpice4's ability to generate arbitrary input stimuli. Shown in table 2 are subcircuits representing various test waveforms taken from IEEE C62.41-1991 for testing surge protection

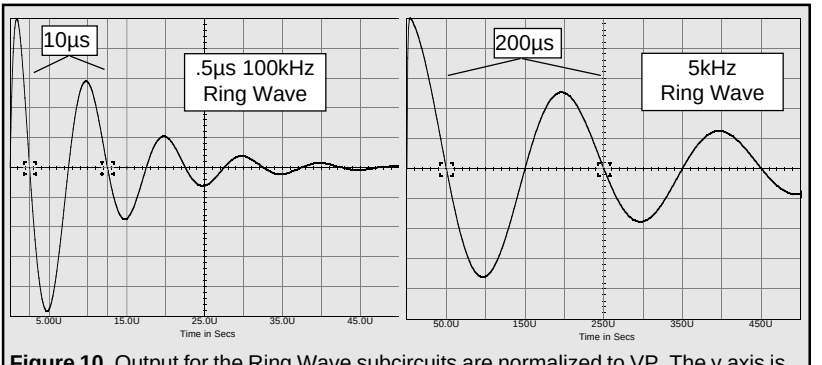



**Figure 10,** Output for the Ring Wave subcircuits are normalized to VP. The y axis is 200mV per division.

```
.SUBCKT RWAVE 2 {A=1.590 T1=0.533U T2=9.788U VP=100}  ; 0.5us 100KHz Waveform
X1 1 TIME
B1 2 0 V = {A * VP} * (1 - EXP( -1 * V(1) / {T1})) * EXP( -1 * V(1) / {T2}) * Cos(6.283185307*100K * V(1))
.ENDS
*******
.SUBCKT WAVE820 2 {A=0.01243E18 T1=3.991U IP=1000}  ; 8/20us Waveform
X1 1 TIME
B1 0 2 I = {A * IP} * V(1)^3 * EXP( -1 * V(1) / {T1})
.ENDS
*******
.SUBCKT WAVE1250 2 {A=1.037 T1=0.4074U T2=68.22U VP=1000}  ; 1.2/50us Waveform
X1 1 TIME
B1 2 0 V = {A * VP} * (1 - EXP( -1 * V(1) / {T1})) * EXP( -1 * V(1) / {T2})
.ENDS
*******
.SUBCKT WAVE101K 2 {A=1.019 T1=3.827U T2=1404U IP=1000}  ; 10/1000us Waveform
X1 1 TIME
B1 0 2 I = {A * IP} * (1 - EXP( -1 * V(1) / {T1})) * EXP( -1 * V(1) / {T2})
.ENDS
*******
.SUBCKT RWAVE5K 2 {A=1.027 T1=0.7356U T2=280.4U VP=1000}  ; 5KHz Ring Wave
X1 1 TIME
B1 2 0 V = {A * VP} * (1 - EXP( -1 * V(1) / {T1})) * EXP( -1 * V(1) / {T2}) * Cos(6.283185307*5K * V(1))
.ENDS
*******
.SUBCKT WAVEEFT 2 {A=1.27 T1=3.5N T2=55.6N VP=1000}  ; EFT Waveform
X1 1 TIME
B1 2 0 V = {A * VP} * (1 - EXP( -1 * V(1) / {T1})) * EXP( -1 * V(1) / {T2})
.ENDS
*******
.SUBCKT TIME  1  ; Requires UIC in the .TRAN statement
C1 1 0 1 IC=0
R1 1 0 1E12
I1 0 1 1
.ENDS
*******
.SUBCKT TIME2  2  ; Does Not Require UIC in the .TRAN statement
A1 1 2 INT  ; Integration Code Model
V1 1 0 1
.MODEL INT INT (In_offset=0 Gain=1 Out_Lower_Limit=-1E12 Out_Upper_Limit=1E12 Out_ic=0
.ENDS
```

**Table 2,** IsSpice4 syntax for a variety of test signal generators. The default parameters are shown in curly braces on the .Subckt line.

devices and circuitry. The subcircuits use IsSpice4's B element and the TIME subcircuit to generate the equations that describe the test voltage. The only required parameters are VP and/or IP. All remaining parameters are taken from the IEEE specification. The effective impedance (Open circuit voltage/Short circuit current) for the sources is not included. This will have to be added according to the conditions under which the sources are used. Figure 10 shows the output for the RWAVE and RWAVE5K subcircuits. An open circuit voltage, Vp, of 170 volts was used and then normalized for the graph. The actual value used will depend on the circuit under test and the conditions specified for the test.

The subcircuit TIME2 uses the new integration code model available in the December ICAP/4 release. This subcircuit duplicates the TIME subcircuit but does not require that initial conditions be set with the UIC keyword on the .TRAN line. This can be very advantageous in some cases.

# Simulating In The 90's

Running SPICE is no longer the same as it was when the program was first introduced. Schematic entry has replaced card decks, interactive simulations that now take only seconds have replaced day long mainframe runs, and real time graphical data processing has replaced crude line printer plots. This is the state of simulation today. Changes brought about by new software products, such as ICAP/4 , have had a profound effect on how engineers simulate circuits.

ICAP/4 is an integrated simulation system that includes 4 modules, each one performing a different function.

- **SpiceNet** Integrated Schematic Entry
- **PreSpice** Model Libraries/Netlist Editing
- **IsSpice** SPICE Simulation/Advanced Analyses
- **IntuScope** Data Processing and Analysis

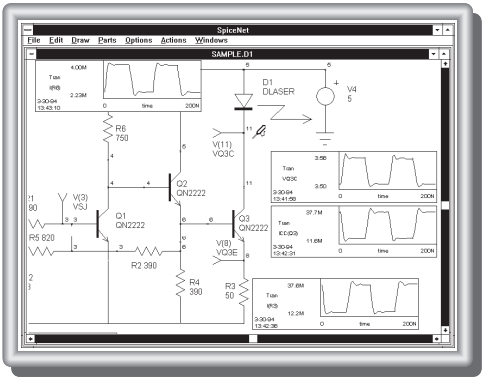
With ICAP/4 you can cut through the toughest circuit design problems with ease, create better products with more functions and higher yields, and explore new concepts. From power to RF to mixed mode, ICAPS allows you to analyze and predict the performance of all types of circuits.

Intusoft has been a leader in full featured design tools since our first product, IsSpice, was released over eight years ago. Our family of software, integrated under the ICAP/4 environment, reduces engineering and manufacturing costs, increases yields, and slashes repair, testing, and design time. The following sections contain detailed information about the ICAP/4 system. They will assist you in discovering the power of ICAPS.

## SpiceNet: Integrated Schematic Entry

**Description:** SpiceNet is a schematic entry program that is designed to be an interactive front-end to IsSpice4. It greatly eases the burden of creating a SPICE netlist by generating a complete netlist, ready for simulation, directly from the schematic. Unlike other schematic packages, which are geared for digital circuits or PCB layout, SpiceNet supports all facets of SPICE. SpiceNet alleviates the editing and syntax headaches allowing you to spend your time creating a better design instead of debugging typos.

**Benefits:** Schematic entry with SpiceNet is designed to be faster than pencil and paper. Most components can be placed on the schematic with a single keystroke. And with all its functions on pull

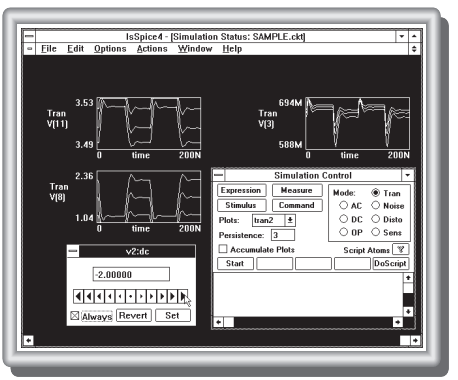



down menus, you can input and simulate your first design in less than an hour. SPICENET has a direct interface to IsSPICE4 allowing waveforms to be interactively cross-probed directly on the schematic. Additionally, the circuit operating point voltages can be updated as component values are changed.

### *Schematic Entry Features*

- Produces a complete SPICE netlist, no editing necessary
- Runs a simulation directly from the schematic
- Interactively cross-probe waveforms by clicking on a node or device
- Change values and resimulate directly from the schematic
- Place parts by part number or from a list
- A Preferred Parts Menu can be defined by the user
- On-line symbol editor plus pre-made symbols for every model
- Automatic subcircuit maker
- Special easy to use pop-up dialogs for SPICE control statements
- Compatible with any SPICE simulator
- Multiple page schematics, Edit several schematics at one time
- Schematics are compatible between versions and platforms
- Cut and paste between different schematics
- Report quality graphics: supports all Windows and Macintosh Chooser output devices

## *IsSPICE: Analog/Mixed Signal Simulation*




**Description:** The new *Interactive* IsSPICE4 program provides a quantum leap in performance over other SPICE simulators. It allows you to explore circuit performance by interactively running different analyses and sweeping any circuit variable. Analyses include AC, DC, Transient, pole-zero, noise, sensitivity, Fourier and distortion analyses. Circuit temperature variations are available for all analyses and individual elements.

**Benefits:** The advanced features of IsSPICE4 allow all types of analog and mixed mode applications to be simulated like: switch mode power supplies, mixed signal ASICs, RF communication systems, interconnect problems, control systems, and mixed domain (mechanical/physical) systems. There are several IsSPICE versions, described next, that vary in speed, circuit size, operating system, and built-in model/analysis support.

- IsSpice4 is 32-bit version of SPICE 3F.2 for Windows, Windows NT and Macintoshs. It supports unlimited size circuits, waveform cross-probing, real time waveform display, *Simulation Scripts and Breakpoints*, and mixed mode simulation.
- IsSpice3 provides the same analysis, model, and real time waveform support as IsSpice4 except that it runs on DOS/ Macintosh systems and is not interactive (SPICE2 batch style).
- IsSpice runs on any PC under DOS or Macintosh. Circuit size is limited to about 200 components. It is based on SPICE 2G.6.

IsSpice3/4 for the PC do NOT require a coprocessor, but one is strongly recommended. All other versions require a coprocessor.

***IsSpice (Analog/Mixed Mode Simulator) Features***

***Analysis and Built-in Models*** (All Versions)

- Elements: Resistors, Capacitors, Inductors, Coupled Inductors, Transmission Lines, Diodes, BJTs, JFETs, MOSFETs (Level 1,2, and 3), Subcircuits, Independent/Dependent sources (SPICE2 polynomials)
- AC, DC, transient, noise, Fourier, distortion, temperature, DC sensitivity

***Additional IsSpice3/IsSpice4 Features***

- Real-time waveform display of voltages, currents and device parameters
- GaAs Mesfets, MOSFETs Levels 4, 5, and 6, Lossy T-Lines, voltage/ current ctrl'd Switches, and Boolean logic expressions. AC sensitivity and Pole-Zero analyses, Temperature variations on individual elements
- Behavioral Modeling: In-line Equations, Table models, If-Then-Else
- Simulation Scripts: a robust scripting language that allows ***Simulation Breakpoints*** and loops of different analyses to be run as a test procedure.

***Interactive IsSpice4 Features***

- Sweep parameters one at a time or in groups
- Add or delete waveforms to the real-time display
- Interactively run any analyses without having to restart the simulator
- Start, Stop, Pause, Change, or Resume any analysis on demand

***Compatibility***

- Works with ALL popular schematic entry programs
- Accepts Berkeley SPICE 2G.6 or 3F.2 syntax

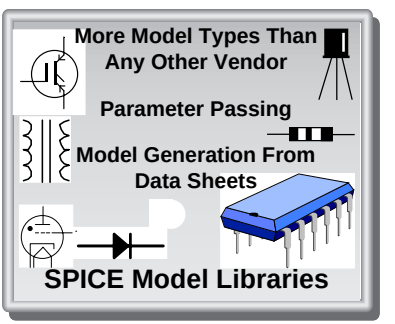
***Advanced Analyses*** (All ICAP packages)

- Monte Carlo Analysis: Statistical yield analysis of circuit performance
  - Randomly vary circuit parameters to test performance
- Circuit Optimization: Automatically find a parameter value to maximize a user defined objective function
- Any circuit performance criteria may be measured including curve families

## *SPICE Model Libraries*

**Description:** ICAP/4Windows and Macintosh include an extensive array of over **4000 SPICE models**.

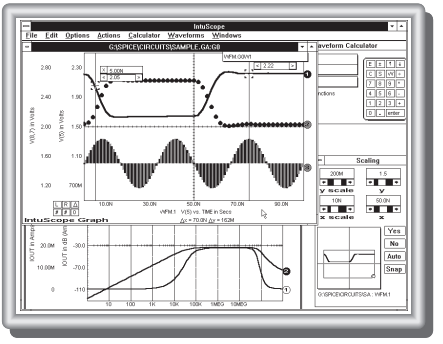
**Benefits:** The SPICE Device Libraries contain a wide variety of models including diodes, zeners, BJTs, Darlingtons, op-amps, comparators, transformers, non-linear magnetics, JFETs, SCRs, IGBTs, Triacs, power MOSFETs, PWMs, SC filters, analog behavioral models, digital logic gates, switches, opto-isolators,



transmission line models, crystals, vacuum tube models and more. Over 100 “Generic Template” models that convert data sheet parameters into SPICE parameters are also included. Models are stored in ASCII text files that can be viewed and edited. A complete list of models is available.

**Note:** The vendor supplied IC libraries (over 1150 models) and the RF Device Library (over 300 models) are available separately.

## IntuScope: Graphical Waveform Processing




**Description:** IntuScope is an interactive graphical data processing program especially designed to display and analyze IsSpice output data. IntuScope can display waveforms from any Berkeley SPICE compatible program, as well as user generated data files.

**Benefits:** IntuScope is more than just a SPICE post processor. It is a very powerful data processing system. It displays data as waveforms and contains a comprehensive set of waveform processing functions and operations.

***Data Analysis Features***

- Displays all circuit voltages, currents, power dissipations and more
- Accepts output from any SPICE program or user generated data files
- Can save any displayed waveform for use as circuit stimulus
- 32-bit version allows large waveforms to be displayed and analyzed
- Various scaling formats include linear, semilog, histogram, and probability
- Multiple graphs with multiple independent scales
- Waveform Operations: RMS, Pk-Pk, Mean, Max, Min, cursors
- Add, subtract, multiply, and divide waveforms
- Math Functions: trigonometric, log, power, $e^x$, algebraic
- Advanced Waveform Functions: Integrate, differentiate, FFT, polynomial regression, filtering, gain/phase margin prop delay, rise/fall time
- Report quality output similar to SpiceNet

## SpiceMod: SPICE Model Generation


**Description:** SpiceMod is a DOS based program that creates SPICE models from data sheet values. It makes models for Diodes, Zeners, BJTs, Darlington BJTs, JFETs, MOSFETs, Power MOSFETS/ BJTs, IGBTs, and SCRs. Although not part of the ICAPS package, SpiceMod is a powerful addition to the models in PreSpice.

**Benefits:** SpiceMod is particularly useful in the circuit design phase because it allows engineers to create SPICE models based on electrical specifications before an actual device is selected. It is also a must for engineers that may have to generate their own SPICE models at a moments notice.

# Additional SPICE Related Products

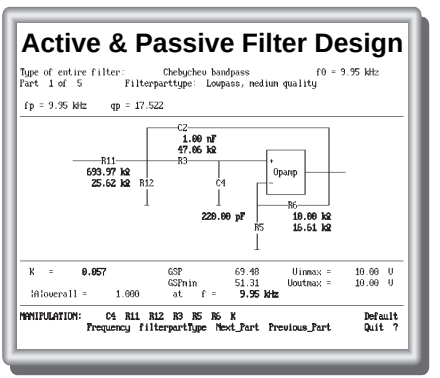
**RF Device Library version 3.0**
**Description:** This is a special SPICE model library for those users performing simulations at or above 200MegHz. It contains models for over 300 different RF devices including bipolar transistors, FETs, MMICs, GaAs Mesfets, PIN Diodes, and RF beads.
**Benefits:** The RF library allows any SPICE program to simulate high frequency circuits using linear and nonlinear AC, DC, and Transient analyses. This capability was not available before because of the lack of quality subcircuit based models. All models are characterized up to their published s-parameter data.

**SPICE Reference Books**
***NEW "SPICE APPLICATIONS HANDBOOK, 2nd Edition"* - Collections of past *Intusoft Newsletters*, 6/86 - 2/94 (34 in all!).**
*"A SPICE COOKBOOK"* - Over 100 practical circuit examples encompassing a wide array of topics (RF, Power, Filters, Digital) and how they were simulated with SPICE.

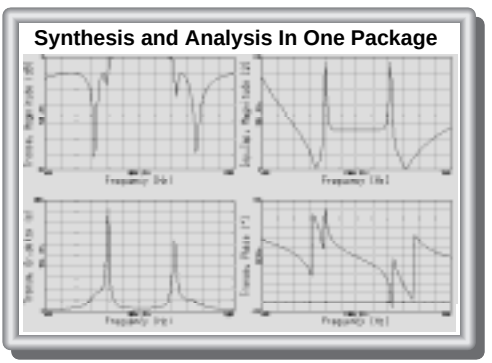
# *FILTERMASTER: Filter Design*

**Active/Passive Filter Design**

**Description:** The FILTERMASTER DESIGN SERIES is a set of PC-based programs used for the synthesis, and analysis of analog LC (lumped element) and active RC filters. Low-pass, high-pass, bandpass, and band-stop filters can be synthesized. Available approximations include: Elliptic (Cauer), Butterworth, Chebyshev, Inverse Chebyshev or, Bessel (for low-pass filters), and two general amplitude approximations.




**Benefits:** The FILTERMASTER DESIGN SERIES includes both synthesis, as well as analysis capabilities, allowing filter topologies and characteristics to be easily compared for the optimal results. Once a filter is designed, it can be transferred directly onto your SPICENET schematic and simulated with ISSPICE.




**Special Interfaces**

- Interface to the SPICENET schematic entry program allowing inclusion of designed filters directly onto your schematic.
- Direct output of subcircuit and stand-alone SPICE netlists.
- Output of component tolerances for use with Monte Carlo statistical yield analysis (passive only).