Intusoft Newsletter

Personal Computer Circuit Design Tools

July 1993 Issue

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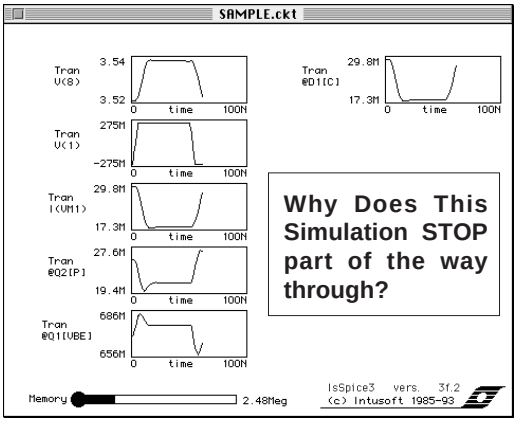
New ICAP/4 Update

ICAP/4 is getting even more powerful. For those engineers looking for simulation tools the ICAP/4 package represents a tremendous value. And since the prices are going up starting September 1, 1993, now is the best time to get the best simulation system.

This update sets a new standard for affordability and performance. It includes a new version of the IsSpice3 program, based on Berkeley SPICE 3F.2. New features include simulation breakpoints, control loops, real time viewing of calculated device parameters such as power dissipation, and greatly enhanced output capabilities. The model libraries in ICAP/4 have also been greatly augmented with over 1300 new models for a wide range of discrete semiconductors and ICs.

In This Issue

New IsSpice3 v3F.2 Let's You See More



Because you asked it too! That's right, the new IsSpice3 v3F.2 includes ***Simulation Breakpoints***. You can ask IsSpice3 to break on a voltage, current, or any of a number of computed device parameters including power dissipation. For example, the statement "**`stop when I(vm1) > 25mA when time > 50ns`**" was used in the simulation to the left. Simulation Breakpoints can be used to test for a variety of conditions including device breakdown, safe operating area, and time dependent events, all while the simulation is running! Some of the other new features are:

continued on page 31-6

New Models Simulate PCB Effects

continued from May 1993 Newsletter

In the May *Intusoft Newsletter* we introduced generic SPICE models for digital input and output stages that can be used with the IBIS (I/O Buffer Information Sheet) specification put forth by Intel. Here, we continue our discussion about the performance of the different subcircuit forms that are available and take a look at how some of the new features in the updated IsSpice3 v3F.2 help to study ground and VCC bounce.

The INTEL IBIS standard has been accepted by a number of IC manufacturers as a viable way to provide modeling data. The only question left to the user is how to turn the data into a subcircuit. In the Part 1 of this article we reviewed two of the IBIS digital buffer subcircuit configurations. IBIS level 1 is based on a topology suggested by Intel. The IBIS level 2 subcircuit uses a similar form, but is built from SPICE 2 elements allowing the subcircuit to run on any version of SPICE. The IBIS level 3 version, shown in Figure 1, also contains SPICE 2 Mosfet and diode models. However, it also takes advantage of IsSpice3's unique mixed mode capabilities to speed the logic processing in the enable section and behavioral modeling features to simplify the pull-up and pull-down structures. IBIS level 3 has been shown to simulate the fastest out of the three subcircuit configurations (See simulation results in Figure 4).

A PC board simulation generally contains three items that must be modeled; the driver, the transmission media, and the load. Fortunately, the IBIS driver model contains the necessary parts to act as a circuit load. Shown in Figure 2 is the output section common to all of the IBIS levels. It contains the pin and package parasitics along with the diode clamps. This stage can be used as a load by connecting an input signal to what was previously the driver's output.

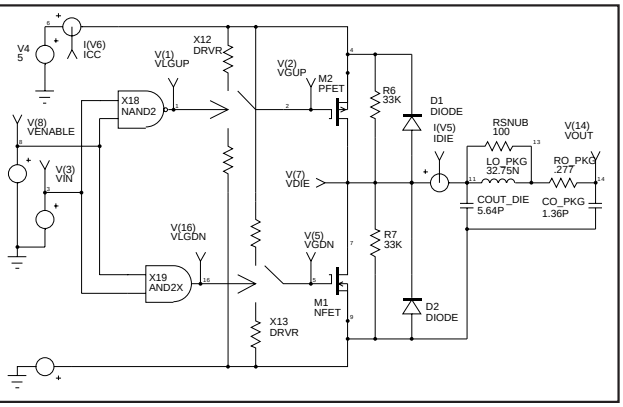


Figure 1, The Intusoft IBIS level 3 subcircuit uses IsSpice3 Boolean logic expressions, behavioral modeling and SPICE 2 diodes/FETS to speed the simulation.

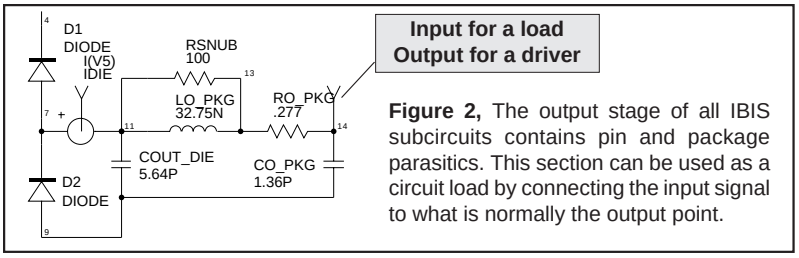


Figure 2, The output stage of all IBIS subcircuits contains pin and package parasitics. This section can be used as a circuit load by connecting the input signal to what is normally the output point.

Benchmarking IBIS Models

The IBIS subcircuits have been tested using three benchmark circuits, shown in Figures 3 and 4. The circuit in Figure 4 is that of the PCI Speedway used in i486 systems. It consists of 9 loads connected to the speedway with 1.5" (vertical) sections of buried microstrip. The horizontal transmission lines represent 1" stripline sections that account for the part-to-part spacing. The connections are modeled using IsSpice3's lossy transmission line:

L/C values in the models are per meter, length is converted from inches to meters

```
.SUBCKT BLINE1 1 2
* Interconnect Model for the Surface Microstrip Stub
* from the PCI Speedway to the component lead
O1 1 0 2 0 LOSSY
.MODEL LOSSY LTRA rel=1.8 len={LENGTH * .0254}M
+ r=0 g=0 l=523NH/m c=76PF/m
* z0 = {(523N/76P)^.5}Ohms, TD = {(523N * 76P)^.5 * (LENGTH * .0254)}s
.ENDS
.SUBCKT BLINE 1 2
* Interconnect Model for the Buried Microstrip PCI Speedway
O1 1 0 2 0 LOSSY
.MODEL LOSSY LTRA rel=1.8 len={LENGTH * .0254}M
+ r=0 g=0 l=723NH/m c=76PF/m
* z0 = {(723N/76P)^.5}Ohms, TD = {(723N*76P)^.5 * (LENGTH * .0254)}s
.ENDS
```

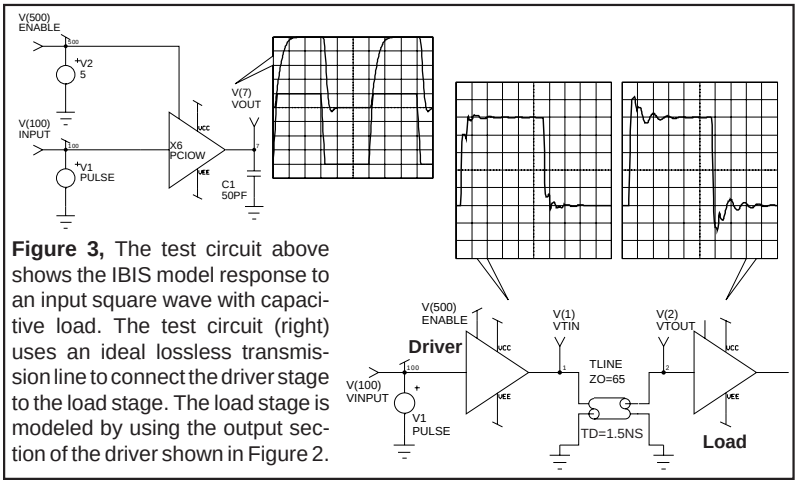
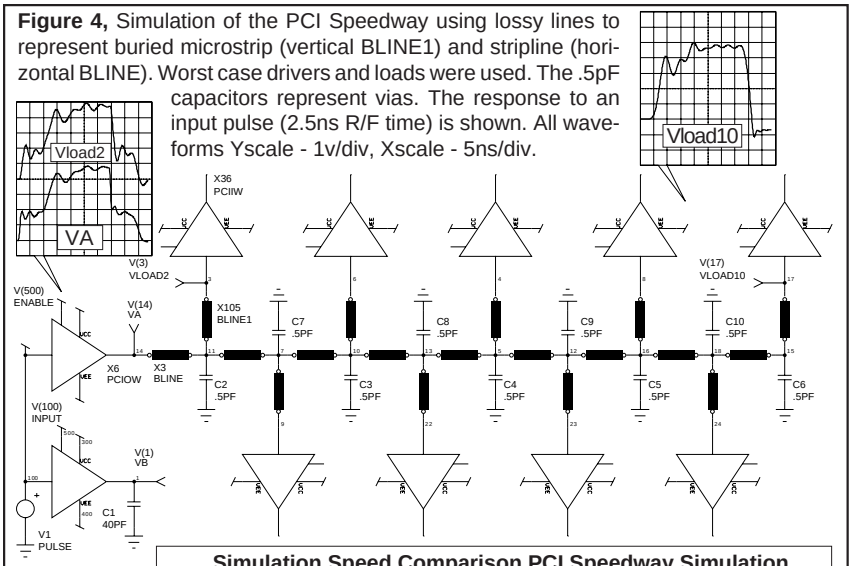


Figure 3, The test circuit above shows the IBIS model response to an input square wave with capacitive load. The test circuit (right) uses an ideal lossless transmission line to connect the driver stage to the load stage. The load stage is modeled by using the output section of the driver shown in Figure 2.

Figure 4, Simulation of the PCI Speedway using lossy lines to represent buried microstrip (vertical BLINE1) and stripline (horizontal BLINE). Worst case drivers and loads were used. The .5pF capacitors represent vias. The response to an input pulse (2.5ns R/F time) is shown. All waveforms Yscale - 1v/div, Xscale - 5ns/div.



Simulation Speed Comparison PCI Speedway Simulation

IBIS1 (SPICE 3 compatible, Table models) -	119.9s, 1048 iterations
IBIS2 (SPICE 2 compatible, FETs/Diodes) -	39.05s, 1168 iterations
IBIS3 (SPICE 3 compatible, FETs/Diodes) -	34.72s, 1096 iterations

New IsSpice3 Features Show Ground Bounce

As circuits become faster, designers must address the effects of package and interconnect parasitics. IsSpice3 is the ideal tool to study the ground and VCC bounce resulting from the added inductance of the leads between the chip and the PC board.

Figure 5 shows a FAST (F240) buffer connected to a 50pF load. The subcircuit, encompassed within the dotted line, contains lead inductance for the I/O and power connections. The new IsSpice3 program gives the user a number of new output capabilities (see pg. 30-6). One of which is the ability to view node voltages or currents through devices without the need for extra voltage sources. When the load is discharged, all of the current flows through the ground lead of the package causing ground bounce. For a switching rate of 3V in 2.5ns, IsSpice3 reports the peak current in the inductor (I(LGND)) to be about 90mA (Figure 6). With a typical lead inductance of 10nH we find the ground bounce at the chip ground to be about ±450mV.

To make a more interesting simulation, a 2 conductor coupled lossy line has been used between the output of the gate and the load. The subcircuit for the coupled line was generated by the utility program "Multidec" included on the newsletter floppy disk. Figure 6 shows the ground bounce inside the buffer (CHIP_GROUND) and the load voltage (VLOAD=V(21)-V(200)).

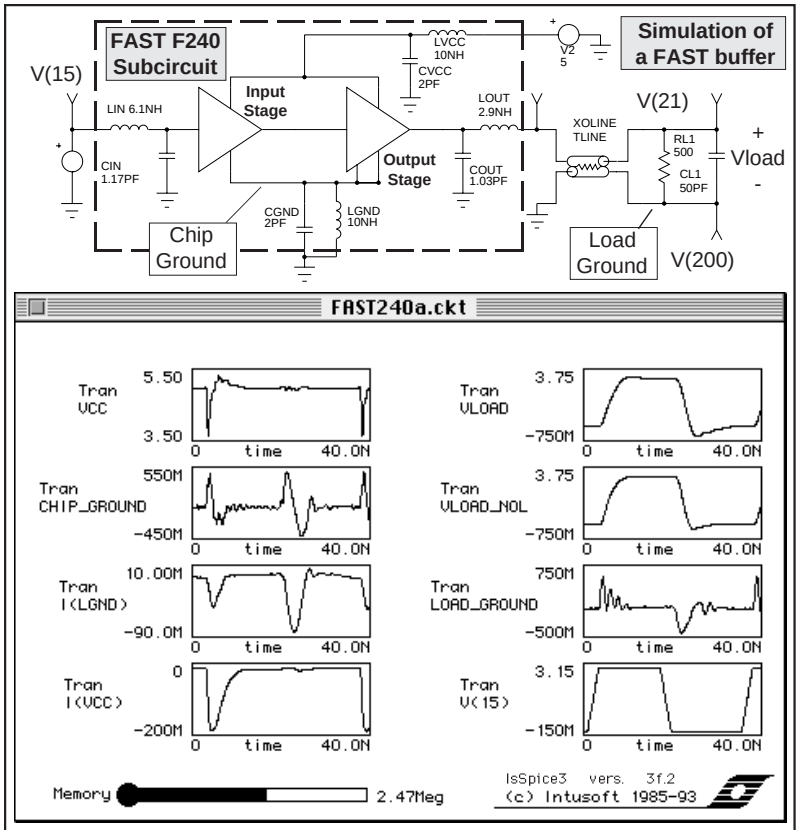


Figure 5, The IsSpice3 real time display now shows currents through subcircuit devices (I(LGND)=Inductor Current) without the need for extra voltage sources.

A VCC bounce is also seen when the load is charged. Node VLOAD_NOL shows the load voltage without the power lead inductances. We can see that VLOAD takes longer to settle out than VLOAD_NOL due to the increased ground bounce. With the help of IsSpice3 it is easy to see how the faster switching rates and lead inductance affect the circuit performance.

The IBIS and Philips models enable designers to tackle circuits that they would not have been able to simulate before. However, it is IsSpice3's powerful features that really make these models useful. Intusoft has created SPICE models for the 82430 PCIset of devices using the three IBIS model variations and models for the Philips ABT, FAST, and ALS logic families. The models are included on the May newsletter floppy disk (available for $20) and have been posted on the CompuServe forum (See page 31-13).

[1] "Package Lead Inductance Considerations in High Speed Applications", S. Hinkle, J. West, Philips FAST Logic, 1989

New ICAP/4 Update

New ICAP/4 & IsSpice3 Features, continued from page 31-1

Computed Device Parameters Access

Now virtually any device parameter can be saved or viewed in real time including device power dissipation, inductor flux, BJT Vbe and FET transconductance, to name just a few. Note: this is not just the simple operating point information that some other SPICE 2 programs put out. This is much more. Operating point information is available, but you can also plot device parameters over time, for example:

.Print tran @d1[p] @q2[vbe] @r1[i] @m5[cgd] @m1[gm]
(Diode power, BJT vbe, Resistor current, MOS G-D Cap., MOS Transcond.)

Enhanced Output Control

The IsSpice3 program allows you to access all of the voltages or currents any where in the circuit. This includes devices in subcircuits. And voltage sources are no longer needed to measure currents in circuit branches. Print expressions containing voltages, currents, model parameters, and a variety of mathematical functions can also be saved to the output file.

Control Loops

With IsSpice3, you can set up a control loop that will perform multiple analyses, check for simulation breakpoints and alter various parameter values after each analysis. There are a variety of control loop types including: ForEach, Dowhile...End, and Repeat.... Some of the commands available inside a control loop are:

AC, DC, TRAN - DC, frequency, and time domain analyses
Alter - Change virtually any device/model parameter
If-Then-Else-End - Conditional branching in a loop
Print - Output any voltage, current, or computed model parameter
Step - Continue a simulation in various increments
Stop - Halt the simulation when certain criteria is meet
Resume - Resume a simulation after a “Stop”

A simple control loop example in IsSpice3:

```
dowhile mean(@d1[p]) < 45m   ; Check the mean diode power dissipation
save @d1[p]                  ; Save the power dissipation as a vector
stop when @d1[p] >= 100m     ; Stop if the peak power dissipation is greater
stop when @r2[res] > 1K        than or equal to 100mW or R2 > 1KΩ
tran 1n 100n                 ; Run a transient analysis
print @r2[res] mean(@d1[p])  ; Print the R2 and mean power dissipation values
print @d1[p]                 ; Print the entire power dissipation vector
alter @r2[res] = @r2[res] + 10  ; Increment R2
end                          ; Do again if the mean D1 pwr. dissip. < 45mW
```

The model libraries in the ICAP/4 package have been updated with over 1300 new models, bringing the total to over 2800. New models include: zeners, diodes, lasers, BJTs, (power and small-signal), JFETs, MOSFETs (power and small-signal), SCRs, triacs, IGBTs, vacuum tubes, digital ICs, and op-amps. Many of these models are not available from any other vendor.

A View To The Future

Faster machines, multi-processor systems, and graphical user interfaces are the way of the future. The very near future. With the introduction of Windows™ NT and the Pentium, MIPS, and DEC Alpha computers, the face of circuit simulation is about to change forever. So what does this mean for SPICE.... In one word, *INTERACTIVE*. Along with new hardware and user interfaces, Intusoft has plans for a new simulation environment. Very shortly, Intusoft customers will get to leave their batch simulation world and enter a totally new environment. Over a year ago Intusoft brought you IsSpice3, the first SPICE simulator to display waveform data in real time. Now, imagine a tool that would allow you to put your hand on a knob that controlled a circuit value. And as you turned the knob you could watch the resulting performance changes; IN REAL TIME. Its not a fantasy, but THE analog/mixed signal design tool you've been waiting for. We all know that the mind is the most powerful design tool. And soon powerful machines coupled with powerful software will give you the freedom to use your best tool.

Join us. It is Intusoft's policy that your investment today carries over to tomorrow. The spaceship for this new world will be leaving soon. And that ship is called IsSpice4. Stay Tuned....

FILTERMASTER - Active Filter Design

continued from May 1993 Newsletter

FILTERMASTER ACTIVE is a PC-based program used for the specification, synthesis, and analysis of active RC filters. It provides both synthesis and analysis capabilities. The integrated graphing routines make it easy to study various design trade-offs during the filter design process. Once finalized, FILTERMASTER ACTIVE provides a finished filter that meets all the design criteria. However, filters are rarely used by themselves. They are normally included with other circuitry which may affect the overall filter performance. In order to allow more advanced filter analyses, FILTERMASTER ACTIVE includes a direct interface to SPICE. FILTERMASTER ACTIVE can output a filter design in the form of a stand-alone SPICE netlist compatible with ANY Berkeley SPICE program. In addition, a filter can also be saved in a subcircuit form that can be called directly from a schematic.

In part I of this article, we used FILTERMASTER ACTIVE to synthesize an elliptic bandpass filter based on the specifications shown in Table 1. In part II, we will transfer the filter design to ISSPICE and perform a Monte Carlo tolerance simulation. Through the Monte Carlo simulation we will investigate the variations caused by passive component tolerances, as well as the op-amp selection.

In order to study the filter's performance using SPICE, the elliptic filter was first saved in a stand-alone netlist format. Next, Monte Carlo tolerances were added to the netlist. Table 1 shows the selected tolerances. The Intusoft generic bipolar input op-amp was used as follows:

```
X1 1 2 3 4 5 OPAMP {GAIN=1500K [GTOL] FT=63MEG [FTOL]
+ IOS=7N [IOTOL] VOS=10U [VTOL] IBIAS=10N [IBTOL] }
```

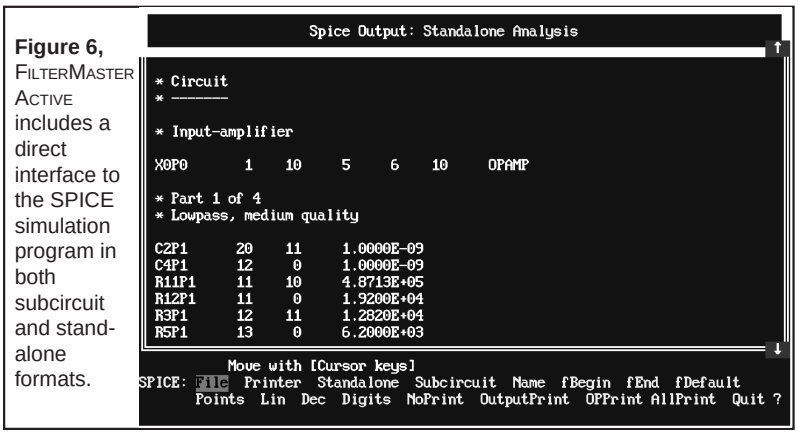


Figure 6, FILTERMASTER ACTIVE includes a direct interface to the SPICE simulation program in both subcircuit and stand-alone formats.

Elliptic Bandpass Filter Specifications			Component Tolerances		
Lower passband edge frequency	:	9.000 kHz	Resistors	:	1%
Upper passband edge frequency	:	11.000 kHz	Capacitors	:	5%
Lower stopband edge frequency	:	8.000 kHz	AVOL	:	40%
Upper stopband edge frequency	:	12.375 kHz	FT	:	30%
Stopband loss	:	50.00 dB	VOS	:	60%
Passband loss	:	<1.00 dB	IOS	:	80%
			IBIAS	:	75%

Table 1, The specifications as they were entered into FILTERMASTER ACTIVE and the component/op-amp tolerances used in the Monte Carlo analysis.

Each op-amp parameter was given its own tolerance as follows:

```
*TOL FTOL LOT=0% DEV=30%   ; FT tolerance 30% ±3 sigma
```

Before the simulation is run, the tolerance evaluation feature in ICAP/4 will set the IOS, VOS, FT, IBIAS, and GAIN parameters on each op-amp to a different value within the ±3 sigma range. Then the parameter passing feature will pass the resulting values into the OPAMP subcircuit and automatically create a different subcircuit for each op-amp that is called.

Once the tolerances are placed in the netlist, the measurements are defined in the INTUSCOPE post processing program. ICAP/4 is not limited to a pre-defined set of measurements. Virtually any circuit performance criteria can be measured. For this Monte Carlo run we recorded the 3dB ripple and bandwidth, and the attenuation at several key frequencies. Curve families can also be gathered, but the curves are often smeared into one another. Superior results are thus gained by making measurements after each run and then formatting them into convenient data sets for later display and analysis.

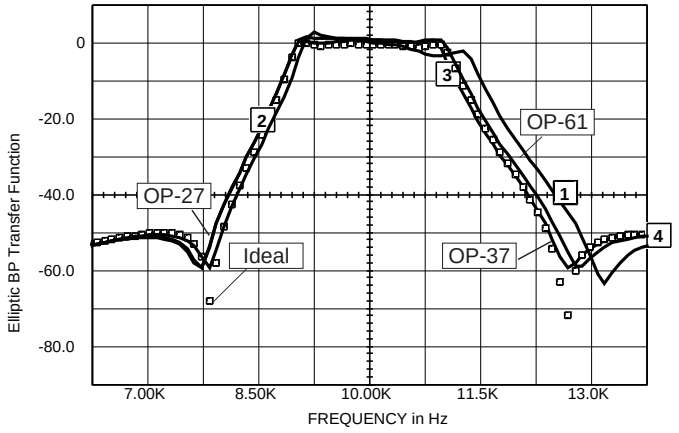


Figure 7, Simulation of the 8th order bandpass filter using various op-amp models. It was discovered that the capacitor tolerances had the most effect on the bandwidth, but the op-amp gain bandwidth product was also critical to good filter performance.

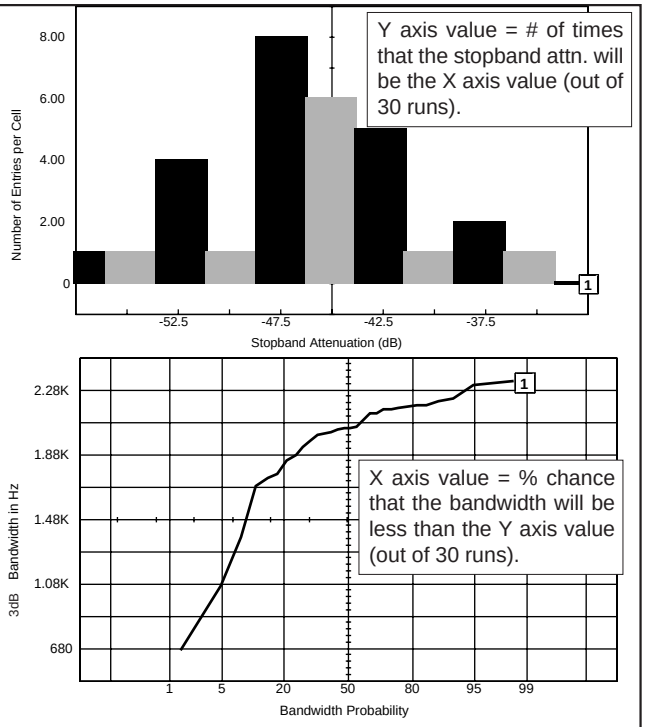


Figure 8, Histogram and Probability plots of the Monte Carlo results using the OP-37. The table below shows the measurements made for 2 runs of 30 cases each, one with an ideal op-amp and the second with the OP-37. Both runs had tolerances on the passive devices.

Elliptic Bandpass Filter: Results of the Monte Carlo Simulation

Measurement	Mean(Ideal)	Std-Dev	Mean (OP-37)	Std-Dev
Bandwidth	1.949 kHz	439.50 Hz	1.948 kHz	354.82 kHz
3dB Ripple	7.916 dB	3.782 dB	10.274 dB	4.492 dB
Attn. @ 8.95kHz	-4.507 dB	3.293 dB	-4.129 dB	3.090 dB
Attn. @ 11.06kHz	-3.771 dB	3.193 dB	-3.637 dB	3.089 dB
Attn. @ 8kHz	-51.577 dB	6.362 dB	-45.27 dB	3.683 dB
Attn. @ 12.38kHz	-49.839 dB	9.756 dB	-45.05 dB	4.854 dB

Two sets of runs, with 30 cases in each, were made to produce the results summarized above. One set was made with an ideal op-amp while the second used the OP-37. It was found that the capacitor tolerances and the op-amp DC gain/GBW value had the most effect on the filter's performance.

FilterMaster Active is the third and newest edition to the FilterMaster Design Series of filter synthesis/analysis programs. There are two passive filter design programs also available: FilterMaster Passive and FilterMaster Professional. The FilterMaster Design series provides affordable, but very powerful, synthesis and analysis capabilities. All FilterMaster programs run on the PC and require 640 KB RAM and DOS 3.0 or higher. FilterMaster Active is available now.

New RF Library Update Adds PIN Diodes

The RF library version 3.0 contains 20 new models for

- **PIN Diodes**
- **Ideal Coupler**
- **GaAs Mesfets**
- **RF BJTs** *(some modeled for Class C operation)*

In addition, over 25 Models for BJTs, MMICs, and GaAs MESFETs supplied by H-P and over 90 RF BJT models from Philips are also included in the update bringing the total number of models in the RF library to over 300. Updates from previous versions are available. The RF Device Library 3.0 will be available July 30, 1993.

PIN Diode Model Attenuates Over Temp.

The most important features of a pin diode are its ability to act as a pure resistance at RF frequencies and to have its resistance varied by a bias current. These characteristics, as shown in Figure 9, make it well suited for mixers, switches, and attenuators. The new pin diode models in the RF Library also include temperature compensation for both DC and AC characteristics and the appropriate package parasitics.

Note: Thanks to **Analog & RF Models**, specialists in the creation of RF device models for their modeling expertise and help with the RF Library.

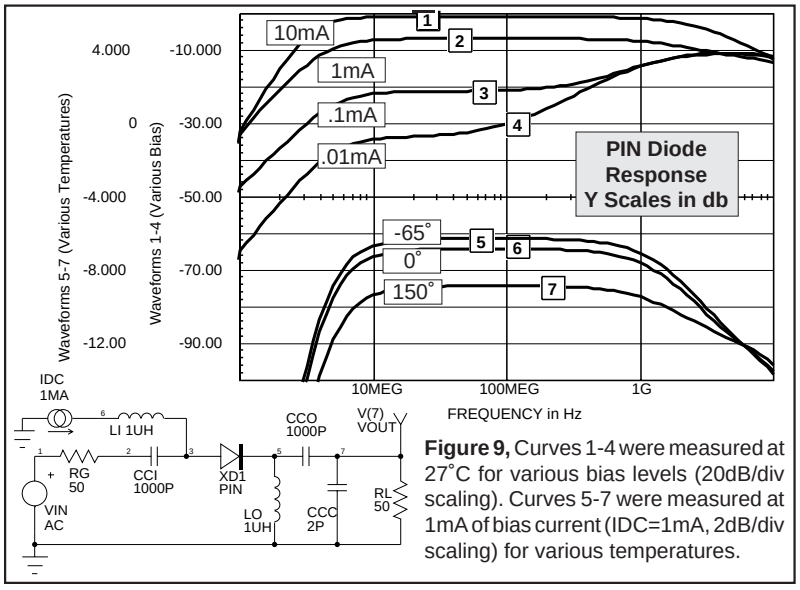


Figure 9, Curves 1-4 were measured at 27˚C for various bias levels (20dB/div scaling). Curves 5-7 were measured at 1mA of bias current (IDC=1mA, 2dB/div scaling) for various temperatures.

Modeling Corner

The Intusoft

Motorola has established new standards for Power Mosfet fabrication with its introduction of the HDTMOS™, (High Cell Density TMOS®) line of devices. In this issue of The Intusoft Modeling Corner we bring you the latest power Mosfet model produced by Motorola for these new devices. These devices feature high current carrying capability and fast recovery with an ultra low Rds(on) under 10mΩ. The newsletter floppy disk contains 3 other models provided by Motorola, as well as over 50 more power Mosfet models developed at Intusoft using the SpiceMod modeling software. On the op-amp modeling front, Motorola has also made available 51 op-amp models for parts like the MC1458 and MC33071.

Burr-Brown has added to their SPICE offering with over 12 new models for Buffers(BUF600), op-amps(OPA502), and inst. amps(INA111). The new op-amp models from both vendors are included on the newsletter floppy disk for subscribers.

```
.SUBCKT MTP75N05G  10 20 30   ;Connections  DRAIN  GATE  SOURCE
* EXTERNAL PARASITICS OF DEVICE *
RD1  2  4  0.0015  TC= 8.73251E-3,7.34669E-6
RD2  4  5  0.0015  TC= 8.73251E-3,7.34669E-6
RS  3  9  0.0030  TC= -5.5296E-3,6.92632E-3
RG  1  8  4
LD  5  10  4.5E-09
LG  8  20  7.5E-09
LS  9  30  7.5E-09
DDS  9  11  DDS1    ; Drain-Source Cap. and Breakdown
RDIO  11  5  0.0026  TC=3.16840E-3,3.17472E-6
DGD  6  4  DGD    ; Drain-Gate Capacitance
RDGD  4  6  1E05
M2  6  4  1  100  MSW1
RSUB1  1  100  1E12
CGDMAX  4  7  2.5E-09
RCGD  4  7  1E05
M3  7  4  1  101  MSW2
RSUB2  1  101  1E12
M1  2  1  3  9  MAIN  W=6.69  L=1E-6
.MODEL  MSW1  NMOS  (LEVEL = 1  VTO  = 0  KP  = 1 )
.MODEL  MSW2  PMOS  (LEVEL = 1  VTO  = 0  KP  = 1 )
.MODEL  MAIN  NMOS  (LEVEL = 3  TOX  = 1E-7  NSUB  = 5.5E15  VTO  = 3.84  PHI  = 0.6
+ UO  = 335.02  KAPPA  = 2.527498E-3  ETA  = 3E-3  THETA  = 0.01  NFS  = 1E12 )
.MODEL  DDS1  D  (  IS  = 7.509945E-12  N  = 1.0332478  BV  = 99.276  IBV  = 0.01  EG  = 1.11
+ XTI  = 4.2125  TT  = 92E-9  CJO  = 4.102016E-9  VJ  = 1.0014842  M  = 0.5098408  FC  = 0.5  )
.MODEL  DGD  D  (  CJO  = 2.43E-9 VJ  = 1.814  M  = 0.884  FC  = 0.5  )
.ENDS
```

Figure 11, The MTB75N05 Power Mosfet model using SPICE 2G.6 syntax. A version using IsSpice3 (SPICE 3F.2) syntax has also been produced by Motorola. The main difference is that resistor temperature coefficients are placed in a resistor .MODEL statement in IsSpice3, i.e.

```
rd1 2 4 0.0015 rd
.model rd r tc1=8.73251E-3
+ tc2=7.34669E-6.
```

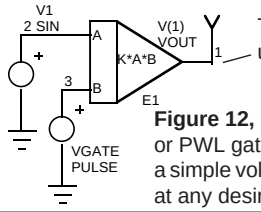
Stimulating Your Circuits

IsSpice provides a variety of voltage and current sources that generate input signals for your circuits. The built-in sources include Sin, Pulse, Piece-Wise Linear, Exponential, and FM. In previous *Intusoft Newsletters* we have also showed how to create AM, 3 phase, and random noise generators. Many more are included in the ICAP/4 software. However, your exact stimulus may not be pre-defined. To solve this dilemma we can often combine one or more generators and some simple analog

behavioral models to produce the desired results. A simple case is shown in Figure 12. In future Modeling Corners we will extend our discussion of stimulus to more complex signals.

Gated Stimulus

```
V1 2 0 Sin 0 120 60 ; Continuous Stimulus
Vgate 3 0 Pulse  0 1 16m 1m
+ 1m  32m; Gating Signal
E1 1 0 Poly(2) 3 0 2 0 0 0 0 0 1 ; Multiplier
```



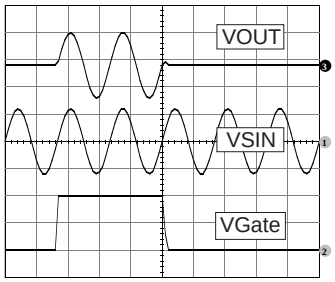


Figure 12, Using a Pulse or PWL gating signal and a simple voltage multiplier, you can turn a continuous signal on or off at any desired time.

Intusoft NEWS: CompuServe BBS

New postings this month on the CompuServe CADD/CAM/CAE forum include a variety of technical articles and application notes including one on simulating connectors. The popular application note ***"Solving SPICE Convergence Problems"*** has also been updated with even more helpful techniques.

To connect with Intusoft you can navigate through CompuServe's computing support menus to reach the CADD/CAM/CAE Vendor forum or type "Go CADDVEN" at any ! point prompt. Then select the "All CADD/CAM/CAE" section. The CompuServe e-mail address is **intusoft@compuserve.com**. Internet users can also send e-mail messages to Intusoft at info@intusoft.com.

Unitrode Seminar Uses Intusoft Tools

Unitrode is offering a series of seminars on Power Supply Design featuring SEPIC converters. Much of the simulation results used in the seminar were generated with Intusoft's circuit simulation tools. For more information on the seminar, along with future dates, contact Unitrode.

EDN Letter Focuses on Circuit Initialization

In a letter to the editor in the May 27, 1993 issue of EDN magazine a Pspice® user reported having trouble running a circuit simulation. The Intusoft technical support staff was contacted to solve the problem and responded with some intriguing and useful solutions. Check out the response for some interesting tips of how to solve SPICE circuit initialization problems (Ask EDN section, pg. 41).