# Intusoft Newsletter

*Personal Computer Circuit Design Tools*

March 1993 Issue




intusoft (310) 833-0710 Fax (310) 833-9658

## Simulating SMPS Designs

The ubiquitous personal computer has made a mess of office power mains. Its characteristic cosine shaped power pulse requires 75% more current carrying capacity than is necessary. Moreover, the turn-on surge is so large that it can cause operational glitches in other equipment. Government regulations will soon force power supply designers to correct this problem. In this article, we will explore some of the design concepts for power factor friendly switched mode power supplies, SMPS. Our motivation here is to show how IsSpice can be used as a high level design tool to explore concepts and develop design requirements before beginning the detailed design phase.

*Continued on Page 29-2*

**In This Issue**



## Intusoft Adds CompuServe® Tech Support

Intusoft is pleased to announce the availability of technical support on the CompuServe® Information Service. To connect with Intusoft you can navigate through CompuServe's computing support menus to reach the CADD/CAM/CAE Vendor forum or type "Go CADDVEN" at any ! point prompt. Then select the "All CADD/CAM/CAE" section to find a variety of new SPICE models, program updates, utilities, demos, and product information. You may also send and receive technical support related mail and files via the forum. Mail messages should be left on the Message section while files can be posted in the Library section.

**After March 29**, as a special introduction to our CompuServe service, an update to the IsSpice3 program will be available at nop charge under the CADD/CAM/CAE forum. The update will introduce some new timestep control options that eliminate the need for manually setting TMAX, some new convergence options, and incorporation of some of the latest Berkeley SPICE 3F.2 additions. The update is available from Intusoft for a fee, but no charge if downloaded from the CADD/CAM/CAE forum on CompuServe. You must have the original IsSpice3 program to use the downloaded update.

CompuServe is a registered trademark of H&R Block Company.

# Exploring SMPS Designs Using IsSPICE

*continued from page 29-1*

First, let's look at the problem. To begin with, the power line impedance must be modeled. With the topology shown in Figure 1, we don't expect the component values to affect current very much, however, the voltage distortion is totally dependent on this configuration. The short circuit impedance was estimated to be equally divided between resistive and inductive components. The high frequency impedance was approximated to be that of free space, hence the choice for the capacitance and the inductor damping. The model could be made more accurate by using test data for a specific case; but the current waveform will not change much and hence the power factor calculation will not be seriously affected by the approximation used here.

The circuit topology of most off-line SMPS uses a full wave capacitor-rectifier with some soft start provisions, mainly to pre-

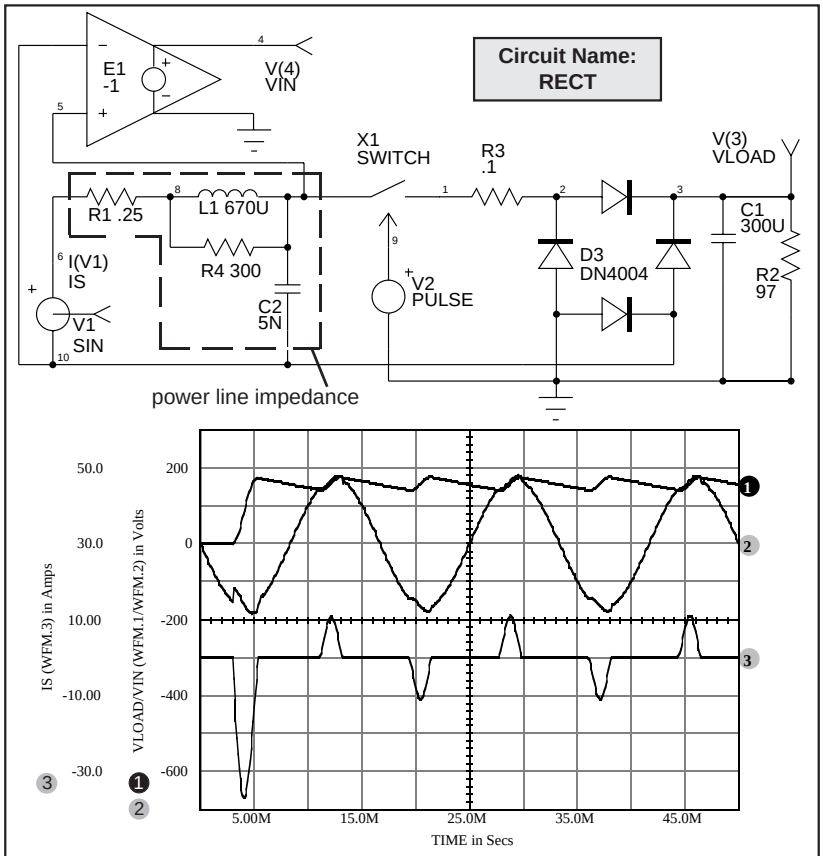


**Figure 1,** Rectifier circuit showing typical SMPS start-up transient. Current is 3.7A RMS, 37A Peak with the peak output ripple at about 5% of the average output voltage.

vent component damage at start-up. The detailed circuit is shown in Figure 1. The graph illustrates the effect of this circuitry on input power along with the capacitor-rectifier voltage. Power factor is defined as the product of the RMS current and voltage divided by the average input power delivered to a circuit. For this circuit; the following measurements were made using IntuScope, a SPICE data post processing program:

| | |
|---|---|
| Iin=3.68 Arms | Vin=120 Vrms |
| Pavg=263 Watts | Power Factor = .596 |

The voltage, VLOAD, in Figure 1, is the unregulated input to the switched mode power regulator. Notice that the peak ripple is about 5% of the average voltage. The regulator must remove this ripple along with other line and load variations.

The object of a power factor correction circuit is to force the input current to be sinusoidally varying and in phase with the input voltage. The input power will then be pulsating at a frequency of twice the input voltage ranging from zero to twice the average input power. The output voltage and current, on the other hand,

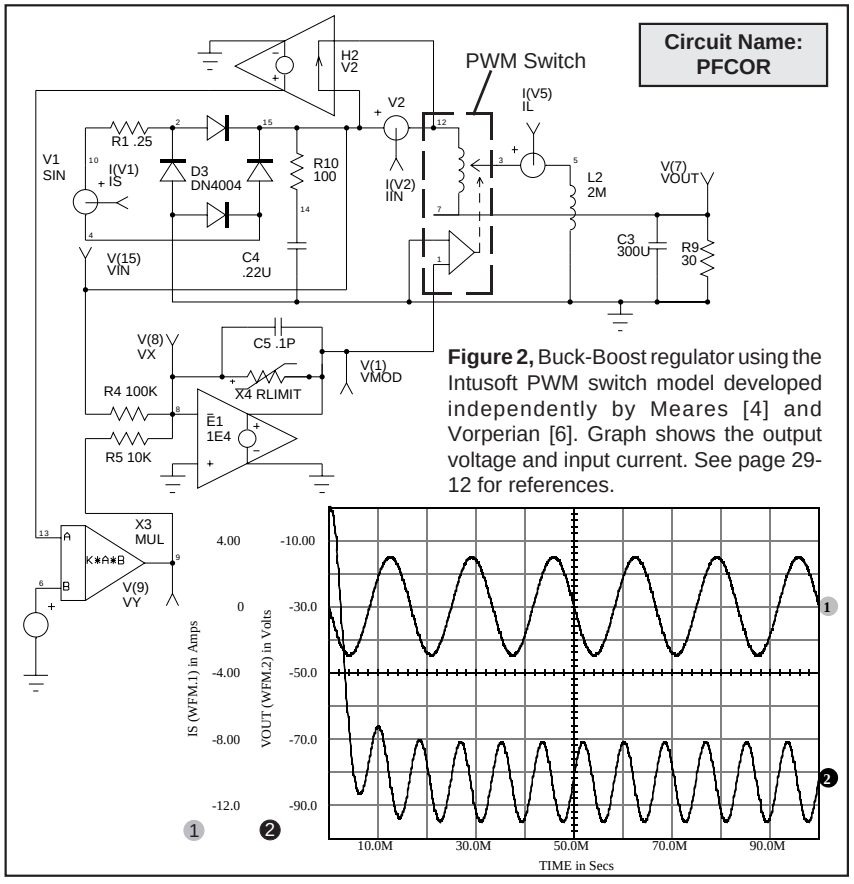


**Figure 2,** Buck-Boost regulator using the Intusoft PWM switch model developed independently by Meares [4] and Vorperian [6]. Graph shows the output voltage and input current. See page 29-12 for references.

must be constant. Therefore, it is necessary to provide reactive elements to store power which can later be used when the input power is less than required.

To accomplish this, the circuit shown in Figure 2 uses a buck-boost regulator to control the input current at a desired level. In this circuit, the pulse width modulator model from the Intusoft library, called PWM, is connected in the buck-boost configuration. To learn more about using this model and review the various PWM topologies, see the article entitled "Average Models For Switching Converter Design" in this newsletter. Here, we will show why the buck-boost configuration has excellent control characteristics for input current.

In Figure 2, the input current is compared with a signal proportional to the rectified input (V(15)) and the resulting error signal (VMOD) is used to control the PWM switch. Notice the use of the limiting resistor (Rlimit) in the error amplifier. This was previously discussed in depth in the September 1992 newsletter. This type of limiter converges and performs better than hard limiters created with Table-type functions. The resulting waveforms show excellent control of the power factor and start-up current. The power factor, as measured using IntuScope, is 1.0. The output voltage magnitude is lower than that of the capacitor-rectifier circuit and the percent ripple has increased from 5% to 15%.

So far we haven't addressed the output regulator. Ideally, the output regulator is a constant power device as is our input regulator. With this configuration we will be using a constant current source to drive a constant current load; therefore, the voltage at the output of our first stage will be difficult to control. Also, the transfer function from input to output will contain those dreaded right half plane zeros, causing problems in designing a responsive controller.

If we select a buck regulator for the second stage, then feedback can be used to control the input current such that the second PWM controller has a 50% duty cycle. If this control loop is very fast, then, the ripple will distort the input current. On the other hand, if it is too slow, the second stage may be presented with too high or too low an input voltage. To overcome these conflicts, the input current requirement can be estimated based on the output power and input voltage. For example, IS $*$ Vs= k $*$ Vset $*$ Ireq; where:

| | | | |
|---|---|---|---|
| IS | = Input current | Vs | = Input voltage |
| Vset | = Desired output voltage | Ireq | = Required output current |
| Vout | = Output voltage | Iout | = Output current |
| k | = Efficiency | | |

| | | |
|---|---|---|
| then, | IS | = k $*$ Vset $*$ Ireq/ Vin |
| however, | Ireq | = Vset / Rload |
| and | Rload | = Vout / Iout |
| finally giving | IS | = k $*$ Vset $*$ Vset $*$ Iout / (Vout $*$ Vin ) |

Several simplifications can be made. First, Vin is assumed to be a constant since it won't vary by more then 15%. Next, since the division by VLOAD may be costly, we should investigate the consequence of making it a constant. The schematic in Figure 3 shows the complete two regulator circuit along with the control mechanism we just discussed. Figure 4 shows the performance comparison when the Vout division is removed. The start-up is somewhat slower, however, the slight performance degradation is not objectionable. Power factor, as measured using IntuScope, was .991. The duty cycle control provided by amplifier E3 makes up for variation in efficiency with load and changes in input voltage. Its authority is limited to 20% of the total control range. This limit will be adjusted as the design progresses as will the compensation component values.

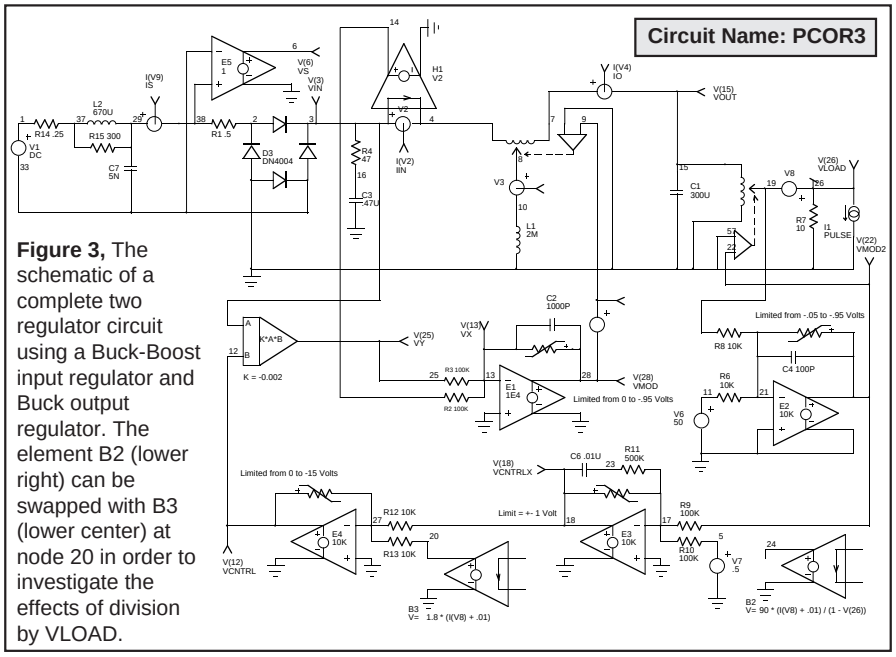


**Figure 3,** The schematic of a complete two regulator circuit using a Buck-Boost input regulator and Buck output regulator. The element B2 (lower right) can be swapped with B3 (lower center) at node 20 in order to investigate the effects of division by VLOAD.

Overall, we have produced a solid framework for an initial design. The next step is to add the input and output noise filters and finalize the compensation circuitry. Then, the power components can be sized based on the currents and voltages found in this simulation. It is important to extract the maximum information from the continuous time model because the actual switched model simulation will run hundreds of times slower. The complete expanded two regulator circuit (PCOR5) is contained on the newsletter floppy disk. Due to space limitations, the final design is discussed in sections. The results are substantially the same as those shown in Figure 4. The power factor is still above 99% although some waveform distortion is beginning to creep in because capacitors were added at the input for noise filtering.

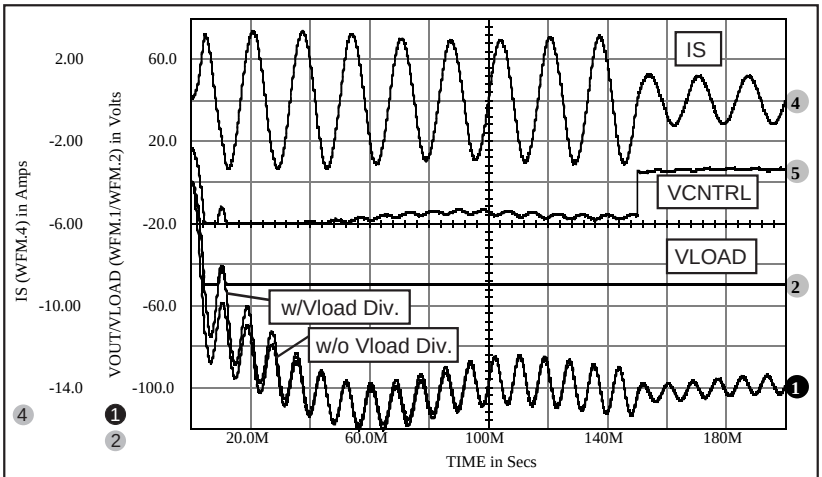


**Figure 4,** Comparison between controllers with and without VLOAD division reveals minimal differences.

The compensation scheme is interesting, especially the outer loop that is used to adjust the output regulator head room. The loop gain for this section is shown in Figure 5 and the schematic of the compensation circuitry for this loop is shown in Figure 6. Notice the technique for making closed loop frequency response measurements. A voltage source is inserted at the point we wish to "cut" the loop, in this case V2. The circuit is excited using only this voltage source. The gain is the difference in the log of the magnitudes and the phase is the difference in phase at each side of the voltage source, VINOL and VOUTOL. The exciting signal must only come from the source we inserted, otherwise the voltages on either side will contain an additional component, making the gain and phase calculations wrong. Capacitor C3 is used to shape the start-up current. If it were to be removed, start-up would be fasted; however, the start-up surge current would be larger. If your final input regulator has current limiting, then this capacitor would be unnecessary.

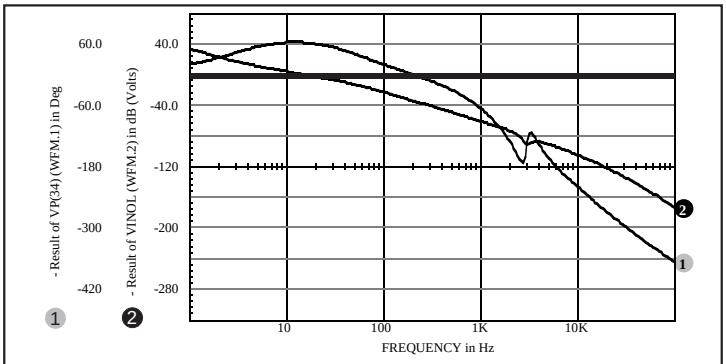


**Figure 5,** Frequency response of the outer loop head room regulator (VINOL/VOUTOL).

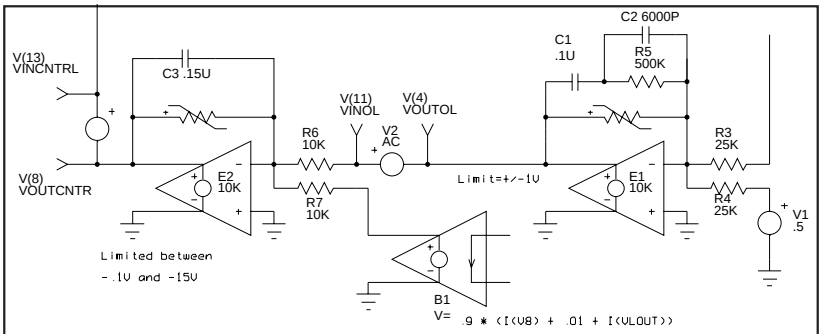


**Figure 6,** Head room regulator section showing the compensation circuitry and technique for calculating a closed loop response.

The output regulator, shown in Figure 7, uses a "poor mans" form of current feedback in order to extend loop bandwidth past the L1-C2 resonance. Current feedback is established by integrating the voltage across L1 using amplifier E1. The voltage at test point VLOAD should also be summed, however, it is approximately a constant and was omitted to reduce complexity. The VLOAD-VLOADIN loop response is shown in Figure 8. In order to help the AC analyses converge rapidly, a .NODESET statement was inserted in order to set the output to 5mV for the DC analysis. The limiters using RLIMIT elements force reasonable operating ranges and also act to aid convergence. Rlimit is made with the new "If-Then-Else" behavioral feature in IsSpice3. Generic parameters include Vmax, Rval, Vmin, and Rmin.

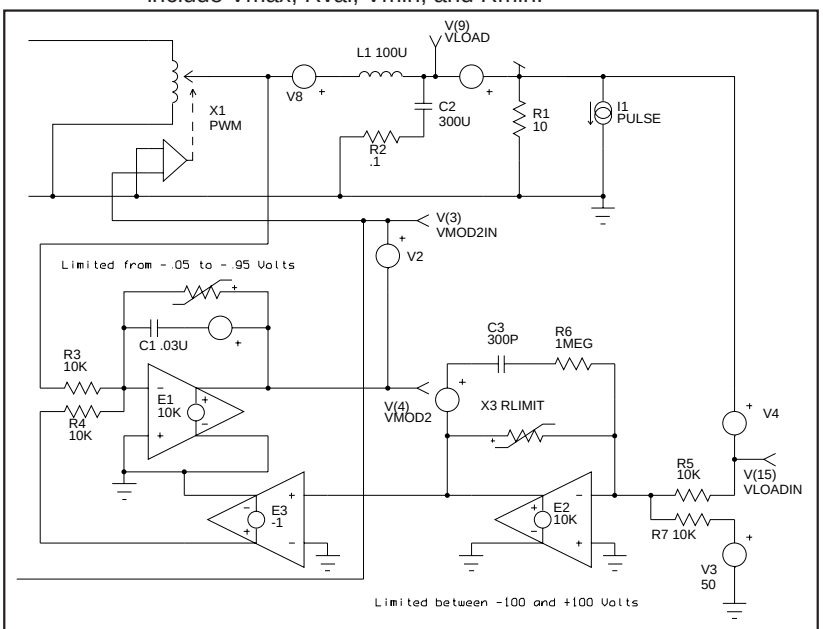


**Figure 7,** The output stage regulator section. The loop is broken at VLOADIN and V4 is inserted as the AC stimulus source.

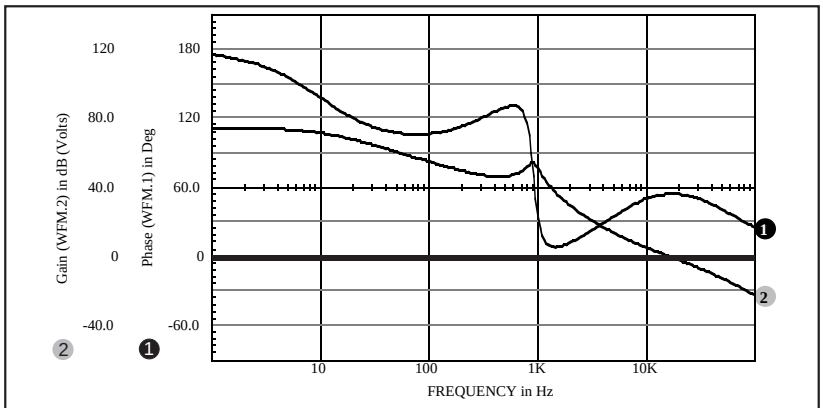


**Figure 8,** The VLOAD-VLOADIN loop response for the buck output regulator section.

The final stabilization and filtering is shown for the input regulator section in Figure 9, with Figure 10 showing the results. In this loop (VMOD-VMODIN), we see the major resonant peaks from the input regulator at 100 Hz and the input filter at 2KHz.

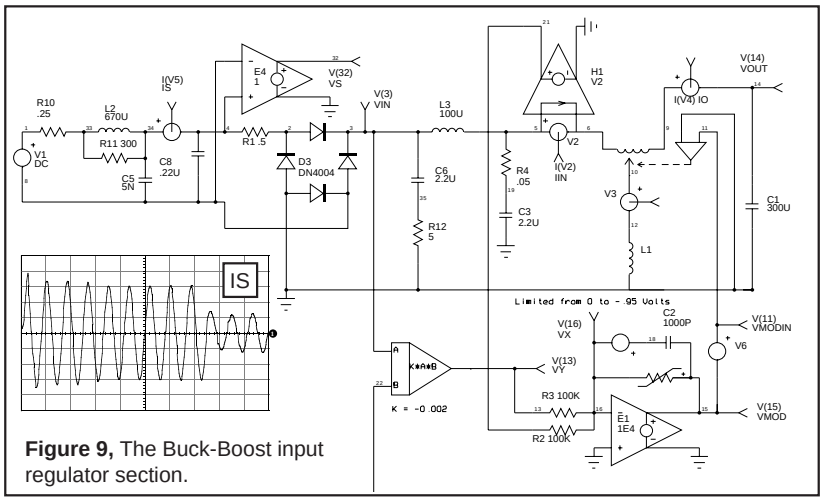


**Figure 9,** The Buck-Boost input regulator section.

While the design is by no means complete, we are confident that the topologies, filters, and control loops are all realizable. It's clear that initialization of the regulators, particularly in relation to housekeeping power turn on must be kept in mind as the design progresses. Selection of the "best" pulse width modulator technology will further refine the control loops. Schematic and SPICE netlists for the circuits shown here, and for switching models of various regulators that can be utilized along with the PWM switch, are included on the newsletter floppy disk. The designs presented here are geared to a 50KHz chopper frequency for the input regulator and 100-200 KHz for the output regulator. Changing these frequencies will affect performance and require revisiting the control loop design.

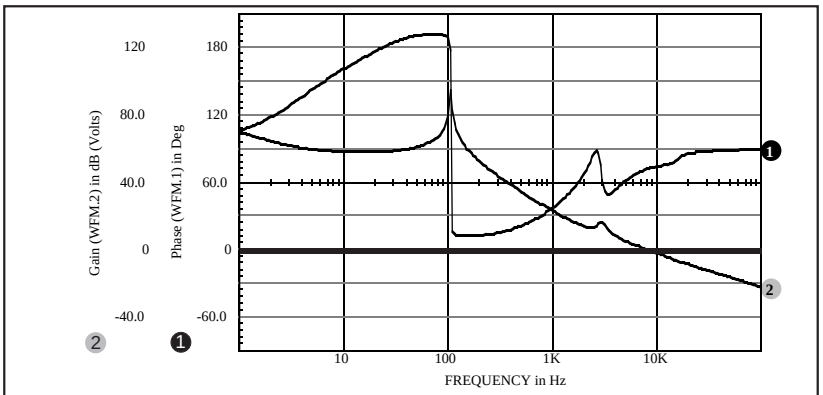


**Figure 10,** The VLOAD-VLOADIN loop response for the input regulator section.

## Average Models For Switching Converter Design

The mathematical basis for modeling switching regulators was established by Middlebrook using state-space average techniques [1]. The implementation using SPICE elements was initially done by Keller [2] and Bello [3] with further enhancements by Meares [4] and Vorperian [6]. The resulting "PWM switch" model can be used for DC, AC small signal, and large signal time domain simulations. The basic PWM model is simply an electrically variable turns ratio DC transformer, hence the pictorial representation. The duty cycle control has two inputs allowing a differential control voltage. It has been shown to provide excellent experimental correlation, even in the neighborhood of the Nyquist frequency (usually 1/2 the switching frequency). In fact, it is possible to predict response past the Nyquist frequency by adding a zero order hold element. But we all know enough to keep our control system bandwidths well below the Nyquist frequency in order to avoid modal nonlinearities. The Buck-Boost and Cuk topologies offer the capability to convert the input voltage to an output voltage ranging from nearly zero to substantially greater than the input voltage. Both topologies, in the transformerless configuration, produce the opposite polarity output voltage from

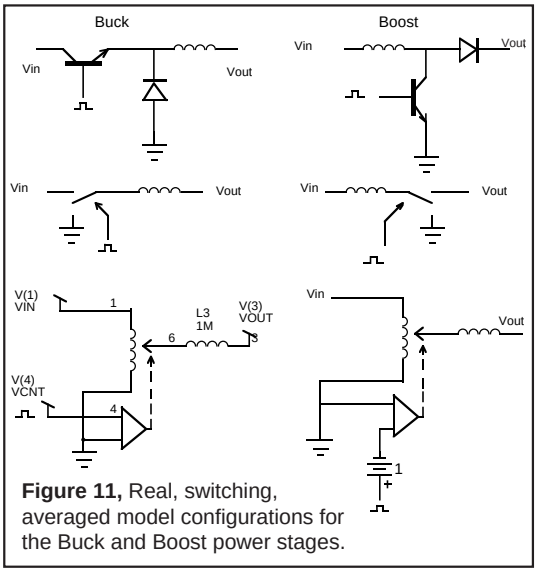


**Figure 11,** Real, switching, averaged model configurations for the Buck and Boost power stages.

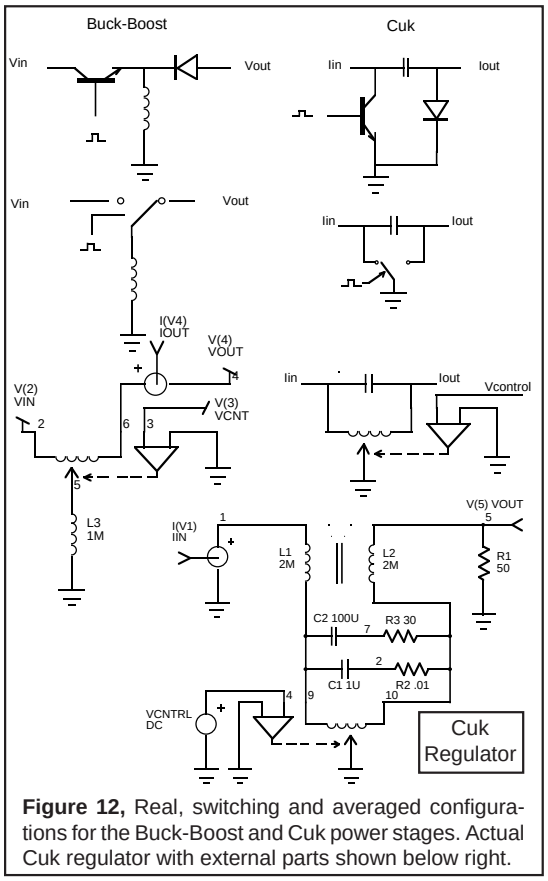


**Figure 12,** Real, switching and averaged configurations for the Buck-Boost and Cuk power stages. Actual Cuk regulator with external parts shown below right.

the input voltage. Since most converters will incorporate transformer isolation within their topology, the polarity inversion is usually not significant.

The duty ratio is defined as the period the PWM switch is turned on divided by the switching period. When forcing switching in both directions, the distinction gets a bit blurred. It is frequently necessary to replace the duty ratio, D, with its inverse, that is Di=1 - D (Fig 11 right bottom), which is the time the opposite switch is on divided by the switching period. For the AC analysis, this will shift phase by 180˚. In the real world, of course you will have to determine the control range and polarity of your PWM in order to account for the scaling and polarity differences between your circuit and the simulation.

## The Basic Power Supply Topologies

There are 4 basic power supply topologies; Buck, Boost, Buck-Boost and Cuk. The most familiar is the Buck regulator. It takes an input voltage from a power source and chops it into a series of pulses. The pulsating voltage is then smoothed using an inductor to produce an average output voltage which is the product of the duty ratio and the input voltage. A typical Buck regulator is shown in Figure 11 using bipolar components. Notice that we always associate one reactive, averaging element with each topology. In the first 3 topologies we are concerned with voltage transformation and allow ripple currents; while the dual CUK topology (Figure 12), transforms current and allows ripple voltage. All 4 topologies require additional filtering at the input and output to make a practical power supply. The Boost configuration shown in Figure 11 is quite different in appearance when viewed as a set of bipolar components; however, when replaced with a “forced” PWM switch representation, it is simply a Buck regulator with the input and the output reversed. Representing each of these configura-

tions using "forced" switching is the same as restricting them to continuous conduction of current in the reactive element. It turns out that this assumption is valid over most operating points of the power electronics we design. This is a very important consideration for simulation because the computational complexity is dramatically increased when discontinuous conduction must be simulated. For the Buck regulator, this occurs at light load; in fact with no load at all the Buck regulator with free wheeling switch commutation fails to provide any regulation, making output and input voltages equal for duty ratios approaching zero. Clearly this condition must be solved in your circuit design, usually with some kind of bleed load; even a status light would work. The point is that the discontinuous conduction region is generally avoided and the continuous conduction region is frequently extended using nonlinear inductors. While Intusoft and the enclosed newsletter floppy provide models capable of transitioning this region[1], we strongly recommend using the continuous model, at least for initial design tradeoff's.

The PWM switch is a versatile element that allows simulation of the majority of features of switching regulators. Its use is essential for performing effective simulations. The floppy disk, included for newsletter subscribers (available to non-subscribers for $20), contains all of the schematics and SPICE circuit netlists in this newsletter, plus models for switching regulators (SG1524, 25, 26, and UA1846 taken from reference [10]). Models for the basic PWM topologies, the PWM switch subcircuit, and an assortment of over 50 models for high power components (Mosfets, BJTs, diodes, SCRs, and IGBTs) are also included.


[1] R. Middlebrook and S. Cuk, "A General Unified Approach to Modeling Switching Converter Power Stages", IEEE PESC, 1976, pp. 18-34

[2] R. Keller, "Closed-loop Testing and Computer Analysis Aid Design of Control Systems", Electronic Design, Nov. 22 1978, pp. 132-138

[3] V. Bello, "Computer Aided Analysis of Switching Regulators Using SPICE2", IEEE PESC, 1980, pp. 3-11

[4] L. Meares, "New Simulation Techniques Using SPICE", IEEE APEC April 1986, pp. 198-205

[5] L. Meares, "Modeling Pulse Width Modulators", Intusoft Newsletter, August 1990

[6] V. Vorperian, "Nonlinear Modeling of the PWM Switch", IEEE Transactions on Power Electronics, Vol. 4, #2, April 1989

[7] V. Vorperian, "Simplify Your PWM Converter Analysis Using The Model of The PWM Switch", VPEC Current, Fall 1988

[8] V. Vorperian, "Simplify PWM Converter Analysis Using a PWM Switch Model", PCIM March 1990 pp. 8-16

[9] L. Dixon, "Spice Simulation of Switching Power Supply Performance", Unitrode Corp., 1991

[10] V. Bello, "Simulation of Switching Regulators Using SPICE2; A Collection of Papers and Subcircuit Models", Meta-Software, 1991


References [9, 10] describe many of the PWM models included on the newsletter floppy disk and add many excellent regulator design examples.

# PreSpice Update/Active Filter Software

The PreSpice module for the Macintosh has been updated to include Monte Carlo Analysis, Parameter Sweeping and Circuit Optimization features. The new version number is 3.2. PreSpice 3.2 will be available on March 29, 1993. Updates from version 3.1M are available.

## Active Filter Design Software has Scaling

FilterMaster Active is a PC-based program used for the specification, synthesis, and analysis of active RC filters. From user entered specifications FilterMaster Active can synthesize the following types of filters: low-pass, high-pass, bandpass, and band-rejection using Elliptic (Cauer), Butterworth, Chebyshev, Inverse Chebyshev, Bessel (for low-pass filters), equal-ripple, and maximally flat approximations. Once a filter is created, graphs of the magnitude, phase, group delay, and pulse/step responses can be viewed. The combination of synthesis and analysis in one program allows various filter topologies and characteristics to be easily compared for the optimal results. A full editing capability allows you to reorder stages, reorder the poles and zeros, and modify component values.

FilterMaster Active includes a special dynamic optimization feature that allows filters to be scaled for different input, output, and op-amp voltage levels. The user can change the maximum input voltage, highest value of the desired output voltage, and the modulation threshold of the op-amp, independently, after the specifications are entered. FilterMaster Active will then automatically recalculate the RC values. This is a unique feature not incorporated in most other active filter design packages and provides a powerful method for component optimization.

Although FilterMaster Active is a stand-alone program, it is still integrated with Intusoft's SPICE based simulation tools. After the design is finished, your filter can be transferred directly onto your SpiceNet schematic and simulated with IsSpice or saved as a stand-alone SPICE subcircuit. Support for a wide variety of output devices (laser, dot-matrix, file formats) is included. **FilterMaster Active will be available April 26.**

# Modeling Corner

The Intusoft

In this issue of The Modeling Corner we will look at creating new switch models in IsSpice3. Subcircuit models for voltage controlled resistors and switches that can be used with any SPICE program have been documented in previous *Intusoft Newsletters*. However, the IsSpice3 program includes a built-in model for both current and voltage controlled switches with hysteresis. Some other PC based SPICE programs include a model for a switch without hysteresis. In order to include hysteresis, additional elements must be used to form a subcircuit. Implementations using a subcircuit approach to achieve variable hysteresis levels are complex and require a much longer time to simulate, thus making them much less efficient than the IsSpice3 switch.

However, the switch in IsSpice3 changes resistance rapidly when threshold is reached. In many cases, a slowly changing resistance is required. Shown below in Table 1 are generic models for several switches whose resistance changes gradually between the on and off states. Since the models are implemented with one or two statements, they run very quickly. Included are models for the types of switches built into the Pspice® program, as well as several others derived from TANH and EXP functions. Subcircuit connections are Out+ (1), Out- (2), Vctrl+ (3), Vctrl- (4).

```
.SUBCKT PSW1 1 2 3 4 {RON=1 ROFF=1MEG VON=1 VOFF=0}
*Pspice® style switch VON > Voff Case
*If VC > VON then RS=RON, If VC < VOFF then RS=ROFF, else RS is as specified in the Pspice® documentation
B1 1 2 I=V(3,4) < {VOFF} ? V(1,2)/{ROFF} : V(3,4) > {VON} ?
+ V(1,2)/{RON} : V(1,2)/ (EXP(LN({(RON*ROFF)^.5}) + (3 * LN({RON/ROFF}) * (V(3,4) - {(VON+VOFF)/2}) /
+ {2* (VON-VOFF)}) - (2 * LN({RON/ROFF}) * (V(3,4) - {(VON+VOFF)/2})^3 / {(VON-VOFF)^3} )))
.ENDS
********
.SUBCKT PSW2 1 2 3 4 {RON=1 ROFF=1MEG VON=0 VOFF=1}
*Pspice® style switch VON < Voff Case
B1 1 2 I=V(3,4) < {VON} ? V(1,2)/{RON} : V(3,4) > {VOFF} ?
+ V(1,2)/{ROFF} : V(1,2)/ (EXP(LN({(RON*ROFF)^.5}) - (3 * LN({RON/ROFF}) * (V(3,4) - {(VON+VOFF)/2}) /
+ {2* (VOFF-VON)}) + (2 * LN({RON/ROFF}) * (V(3,4) - {(VON+VOFF)/2})^3 / {(VOFF-VON)^3} )))
.ENDS
********
.SUBCKT TANHSW 1 2 3 4 {RON=1 ROFF=1MEG VON=1 VOFF=0}
* TANH Function
B1 1 2 I=V(1,2)/ ({ROFF}-{.5*(ROFF-RON)} * (1 + V(5)))
B2 5 0 V=TANH({(VOFF+VON)/(VOFF-VON)} + (2 * V(3,4)/{VON-VOFF}))
.ENDS
**********
.SUBCKT GSW 1 2 3 4 {RON=1 ROFF=1MEG VON=1 VOFF=0 SC=15.708}
* Gudermannian Function
B1 1 2 I=V(1,2)/({.5 * (ROFF+RON)}-({2 * (ROFF-RON)} / PI *
+ (ATAN(EXP({SC} * ((V(3,4)/{(VON+VOFF)/2}) - 1))) - PI/4)))
.ENDS
**********
.SUBCKT EXPSW 1 2 3 4 {RON=1 ROFF=1MEG VON=1 VOFF=0 SC=20}
* Fermi Probability Function
B1 1 2 I=V(1,2)/({RON} + ({ROFF-RON}/(1 + EXP({SC} * (V(3,4)/{(VON+VOFF)/2} - 1)))) )
.ENDS
```

**Table 1,** Using the behavioral modeling features of IsSpice3, including in-line equations and an If-Then-Else statement, a wide variety of nonlinear switches can be created. Functions taken from IEEE Circuits and Devices Magazine, Sept. 1991, pp 9-37.

Pspice is a registered trademark of Microsim Corp.