Intusoft Newsletter

Personal Computer Circuit Design Tools

September 1992 Issue

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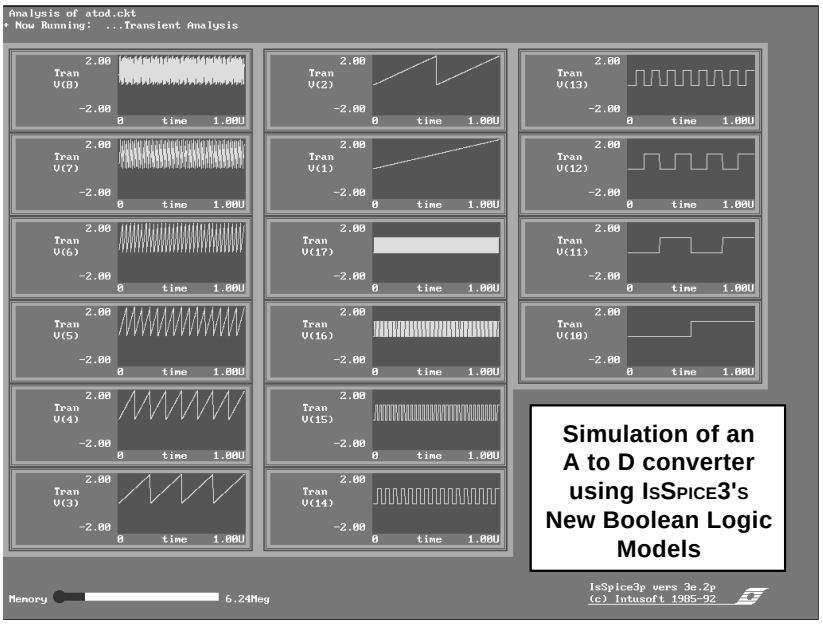
IsSpice3: The Next Generation

Intusoft is going to change the way you feel about the cost and performance of personal computer based circuit simulation.

- **With Workstation Features:** Real Time Waveform Display, Mixed Mode Simulation, Analog Behavioral Modeling
- **With New Models:** Mesfet, Mosfet (BSIM 1 and 2, Level 6), Lossy Transmission Lines, built-in Switches
- **With New Analyses:** Pole-Zero, Temperature, Distortion

All included with IsSpice3, a completely new version of IsSpice based on the Berkeley SPICE 3E.2. Look inside for more details and information.

In This Issue



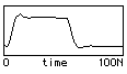
Simulation of an A to D converter using IsSpice3's New Boolean Logic Models

IsSpice3: The Next Generation

The new IsSpice3 program provides a quantum leap over SPICE 2 based simulators. It is the first commercially available version of SPICE to be based solely on the latest version of SPICE from Berkeley, version 3E.2. It is not a version of SPICE 2G.6 that has been augmented with parts of SPICE 3, as so many other vendors have done. Although IsSpice3 uses virtually the entire SPICE 3E.2 program, it is not a straight port.

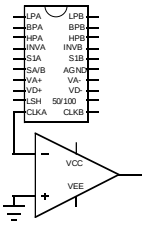
Intusoft has greatly enhanced the program over and above the Berkeley 3E version. Some of the features unique to Intusoft's implementation include:

Real Time Waveform Display



IsSpice3 draws waveforms from the DC, AC, Noise, and Transient analyses as the simulation runs (See Page 26-1). This allows the user to see how the simulation is progressing and decide whether to continue or abort the run. This feature is available on all platforms. (386/486 based PCs and compatibles, Macintosh, and NEC 98-series computers)

Mixed Mode Simulation



Mixed Mode and digital logic simulation capability is now available using three levels of modeling: exact transistor topology, behavioral, and the new built-in Boolean logic expressions. This feature allows analog and digital circuits to be simulated at the same time.

Analog Behavioral Modeling Extensions

New Analog Behavioral Modeling features include: in-line equations using algebraic, trigonometric or transcendental operators, node voltages and voltage source currents, as well as, an If-Then-Else function useful in a variety of applications (switches, digital logic operations, comparators, limiters, etc.)

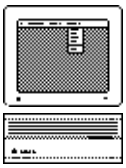
Advanced Memory Allocation and Control

Extended memory usage is now adjustable by the user. A virtual memory option allows simulations to access up to 32 megabytes of memory by using either RAM, hard disk space, or a combination of both.

Berkeley SPICE 2 Compatibility

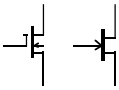
IsSpice3 is compatible with Berkeley SPICE 2 input and output syntax. It can run virtually all past designs without any modifications. SPICE 2 dependent source (E, F, G, H elements) polynomial syntax is automatically converted to the new nonlinear dependent source (B element) providing backward compatibility with all Intusoft and vendor supplied op-amp model libraries.

In addition to all of the major analysis types and built-in models of previous IsSpice versions, IsSpice3 also adds:



More Hardware/Operating System Support
IsSpice3 runs under DOS, Macintosh, Windows 3.1 (Himem.Sys compatible) and OS/2 (DOS Window). A Windows NT version of IsSpice3 is currently in Beta site. On the PC, graphics support is included for EGA through XGA resolution (1024x768).

New Models
New built-in models include: 3 new Mosfets (BSIM 1, BSIM 2, and Level 6), GaAs Mesfet (Based on the Statz model), lossy transmission lines, distributed lumped RC transmission line, and voltage and current controlled switches.



Improved Models
The lossless transmission line model has been completely redone. Highly efficient algorithms now enable IsSpice3 to simulate circuits with large numbers of transmission lines more than 100 times faster than SPICE 2. The Mosfet model has also been improved, eliminating many of the “timestep too small” problems.

New Analysis Capabilities
IsSpice3 allows an independent temperature setting on various elements. This allows the user to simulate a “hot” component that has a different temperature than the rest of the circuit. A new Pole/Zero transfer function analysis is also available.

Improved Analysis Capabilities
The distortion analysis has been rewritten to include distortion effects for all active components. The convergence of IsSpice3 has been greatly improved due to the addition of new Gmin and source stepping algorithms and improved program defaults (No Limpts/ITL5 parameters required).

Input Netlist Flexibility
IsSpice3 accepts upper or lower case entries, greater than 8 character model/subcircuit/reference designation names and negative capacitor and inductor values. Names can also be used in place of node numbers. IsSpice3 can be driven from virtually any schematic package that puts out a Berkeley SPICE 2 netlist.

Macintosh Speed Comparable to 80486
The speed of the Macintosh version of IsSpice3 has increased by 200 to 1000% over past versions of SPICE. IsSpice3 is compatible with the Quadra’s hardware cache.

IsSpice3 is truly the next generation in SPICE simulation software. It is ready to take you beyond your current simulation limits; with the latest state of the art features and a price you can afford.

IsSpice3 Enables New Applications

There is no doubt that the new analog behavioral and mixed mode capabilities in IsSpice3 will greatly impact the way many systems and components are modeled. The ease and flexibility that these techniques provide over traditional modeling methods will result in vastly improved simulation performance, speed, and convergence properties.

The new analysis and modeling features in IsSpice3 will open up many simulation boundaries that were beyond the reach of SPICE 2 based programs. Simulating new applications like: mixed analog and digital ICs, PCB transmission line effects and high speed board layout, A/D and D/A circuits, and mixed domain (mechanical/electrical) systems is now possible. In future newsletters, we will explore the new features and capabilities that IsSpice3 provides in depth. Shown next are three brief examples depicting analog behavioral modeling (ABM) and mixed mode features.

Analog Behavioral Modeling: In-Line Equations

Since being introduced in SPICE 3A.7, equation based modeling has quickly emerged as the simplest method for novice SPICE model builders to add functionality. The analog behavioral capabilities of IsSpice3 include in-line equations using algebraic, trigonometric, and transcendental operators, along with node voltages, and voltage source currents.

The following example is discussed fully in "A Spice Cookbook". Simulation of the antenna beam pattern received by an observer can be accomplished with transmission lines in IsSpice. However, this approach can be rather time consuming because of the large number of T-lines needed. A superior method involves using mathematical representations.

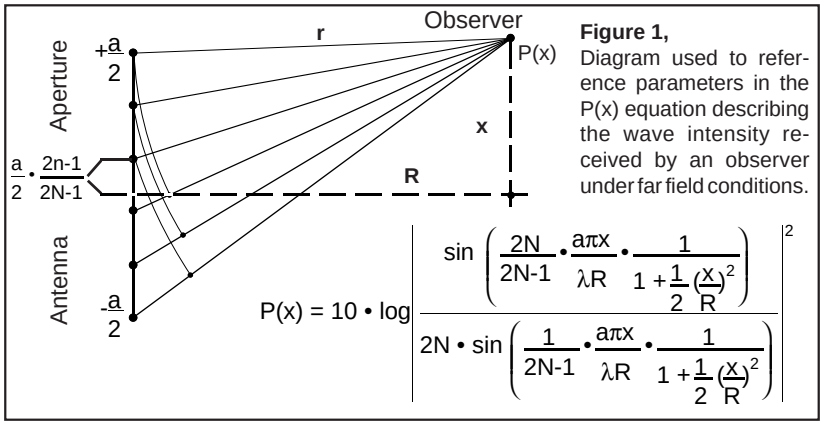


Figure 1,
Diagram used to reference parameters in the P(x) equation describing the wave intensity received by an observer under far field conditions.

Before IsSpice3, P(x) was most easily calculated using a BASIC program. Referring to Figure 1, the equation for P(x) can now be implemented using IsSpice3's new nonlinear dependent source, (the B element) which allows equations to be entered directly.

```
BTOP PXNUMER 0
+V=SIN((2*V(N)*V(A)*PI*V(X))/
+ ((2*V(N)-1)*V(L)*V(R)
+ *(1+.5*(V(X)/V(R))^2)))
BBOT PXDENOM 0
+V=2*V(N)*SIN((V(A)*PI*V(X))/
+ ((2*V(N)-1)*V(L)*V(R)
+ *(1+.5*(V(X)/V(R))^2)))
BOUT PX 0 V=10*LOG(ABS
+ (V(PXNUMER)/V(PXDENOM))^2)
```

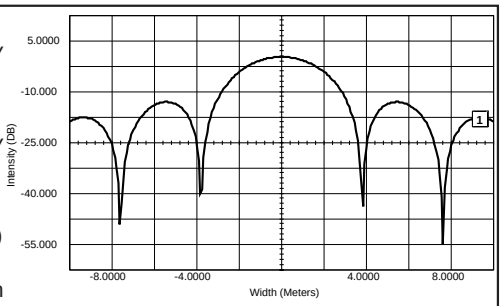


Figure 2, In-line equations for an antenna far field response using the new IsSpice3 B element. The equation was broken into three parts for clarity.

Simulation using equations provides a number of advantages. First, the resulting intensity can be used as input stimulus to a receiver circuit. In addition, all of the constant parameters, such as the x axis distance, R, can become variables, providing for a much more interesting simulation.

Mixed Mode Simulation: Boolean Logic Expression

In IsSpice3, mixed mode simulation is handled on three levels:

- With exact subcircuit models that use the actual transistor topology of the integrated circuit,
- With macro models that use behavioral modeling techniques such as polynomial functions to emulate logic gates, and finally,
- In-line Boolean logic expressions, a new capability that speeds up simulations by an order of magnitude.

Each of these methods has its merits and target applications. In fact, many simulations call for the combination of all three approaches. However, the ability to insert Boolean logic expressions into a SPICE netlist is not available in most other SPICE simulators. Yet, it is one of the most powerful methods for integrating logic functions in an analog simulator.

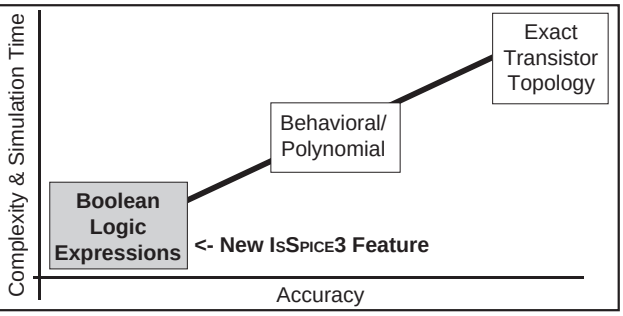


Figure 3, The new IsSpice3 program supports all three levels of digital gate representation allowing varying degrees of mixed mode simulation accuracy and speed.

Boolean expressions produce a continuous set of possible logic states that are continuously evaluated during the simulation. This allows digital gate responses that are as accurate as transistor level simulations and free from unknown states.

Simulating A Binary Full Adder

To illustrate the power and flexibility of Boolean logic expressions, a 2-bit binary full adder, similar to the TI SN7482, was simulated. The entire range of input states were simulated under four modeling scenarios; Boolean expressions of the entire circuit (Figure 5), simple boolean expressions for each individual gate, individual boolean gates with an RC delay added to the output of each gate, and behavioral gates using polynomial expressions. The simulations produced comparable results as shown in Figure 4, with the Boolean expressions running an order of magnitude faster than the digital gates using behavioral method.

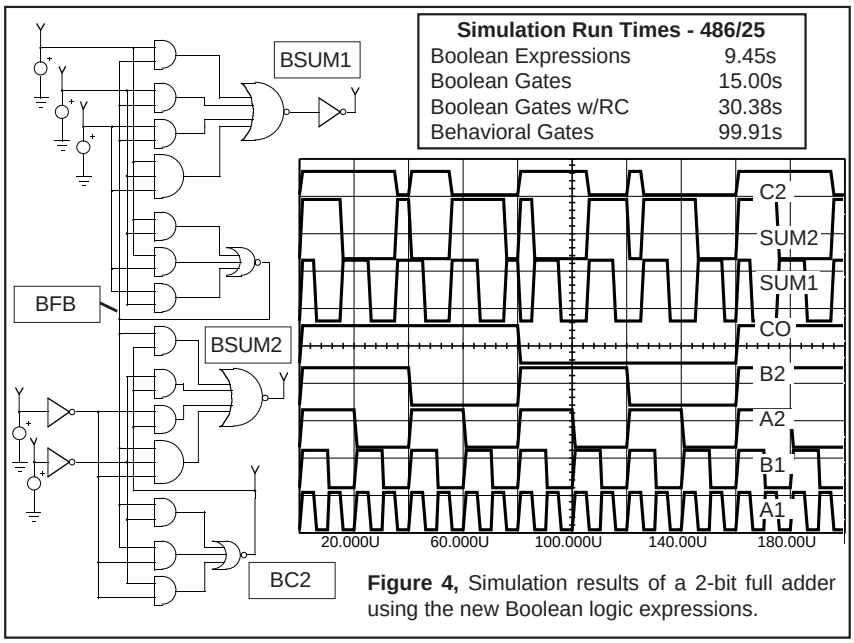


Figure 4, Simulation results of a 2-bit full adder using the new Boolean logic expressions.

Mixed Signal Simulation: If - Then - Else Expressions

IsSpice3 contains a flexible If-Then-Else function using syntax borrowed from the C programming language. It is useful for making very efficient limiters, comparators, and logic gates. If-Then-Else clauses can also be used as switches capable of redirecting the flow of simulation. In Figure 5, the subcircuit representing one bit of an A/D converter is shown. The statement `b1 bin 0 v= (v(in) > 1) ? 1 : 0` can be read as "If the voltage at node IN is greater than 1V, then the voltage at BIN equals 1V,

Boolean expression describing 2 BIt Binary Full Adder

```
BSUM1 SUM1 0  V= (V(C0)&V(FB)) | (V(A1)&V(FB)) |
+ (V(B1)&V(FB)) | (V(C0)&V(A1)&V(B1))
BSUM2 SUM2 0 V= ~((V(FB)&V(C2)) | (~V(A2)&V(C2)) |
+ (~V(B2)&V(C2)) | (V(FB)&~V(A2)&~V(B2)) )
BC2  C2 0 V= ~((V(FB)&~V(A2)) | (V(FB)&~V(B2)) | (~V(B2)&~V(A2)))
BFB   FB 0 V= ~((V(C0)&V(A1)) | (V(C0)&V(B1)) | (V(B1)&V(A1)) )
```

Subcircuit using If-Then Else expression describing an A/D

```
x1 1 2 10 adc
.subckt adc in out bin
b1 bin 0 v= (v(in) > 1) ? 1 : 0     <-- If Then Else function
b2 out 0 v= 2*(v(in) - v(bin) * 1)
.ends
```

Figure 5, The boolean expressions that form the full adder and If-Then-Else show how easy mixed mode simulations can be implemented in IsSpice3.

else, the voltage at BIN equals 0V. Several levels of else-if clauses can be inserted. The results of the simulation of an 8 bit A/D converter are shown on the front cover of the newsletter.

In summary, IsSpice3 is the first commercially available version of Berkeley SPICE 3E.2. It runs on PC and Macintosh computers. IsSpice3 is not simply a port of SPICE 3E.2. It is the next generation SPICE simulator encompassing real time waveform display, mixed signal simulation capability, state of the art models, and advanced analog behavioral modeling features that will allow you to boldly go where no SPICE simulator has gone before.

Note: New models developed using IsSpice3 syntax will initially be available to newsletter subscribers. At a future date, the models will be included in an update to the PreSpice Model Libraries.

IsSpice3 Availability

IsSpice3 will be available as of September 15. Upgrades from previous versions of IsSpice are available. IsSpice3 is included in the ICAP/4 simulation system. Unlike competing solutions costing over 4 times as much, the ICAP/4 system provides the full set of SPICE capabilities along with schematic entry, analog behavioral modeling, extensive model libraries, and mixed mode simulation. If your wondering why our prices are so reasonable, maybe its time you asked the competition why their prices are so high.

IsSpice3 Hardware/Software Requirements: *Computer:* 386/486 PC, Macintosh, and NEC 98-series computers, hard disk, and a coprocessor. *Memory:* At least 2 megabytes of extended RAM. *Operating System:* DOS 3.3 and up, Macintosh, Windows 3.1 (Himem.Sys compatible) and OS/2 (DOS Window).

Solid State Relays and Switches

Part II

In part I of this application note (June '92) we explored the creation of solid-state relays (SSR) and switches with various levels of modeling complexity. In part II, we will explore the new built-in switches in IsSpice3 and create a model for the CD4066B CMOS analog switch. Then, we will demonstrate a sample-and-hold circuit using several switch models.

New Switch Models in IsSpice3

Creating a switch in SPICE 2 necessitated the use of a subcircuit with a polynomial controlled source. Although the switch impedance was voltage controlled, and it ran well, it can not automatically switch based on an input level, nor does it have any hysteresis. In IsSpice3, voltage and current controlled switches with these features are built into the simulator.

The response for the IsSpice3 switch is shown in Figure 6. It is used like an active device, with a call line and a .model statement. For example, "**`S1 10 1 6 0 Smod`**" and "**`.Model Smod Sw Ron=45 Roff=10Meg VT=4.5`**" defines the switch used later in the sample-and-hold simulation.

The CD4066B, CMOS bilateral switch, was developed in a manner similar to the DG200. Data sheet information was feed into the SpiceMod modeling spreadsheet program. After obtaining preliminary Mosfet models, a subcircuit using the exact transistor configuration of the device was created. Once configured, simulation of data sheet supplied test circuits allowed characterization of ron, total harmonic distortion, I/O leakage currents, and the propagation delay. The final subcircuit is listed in Table 1.

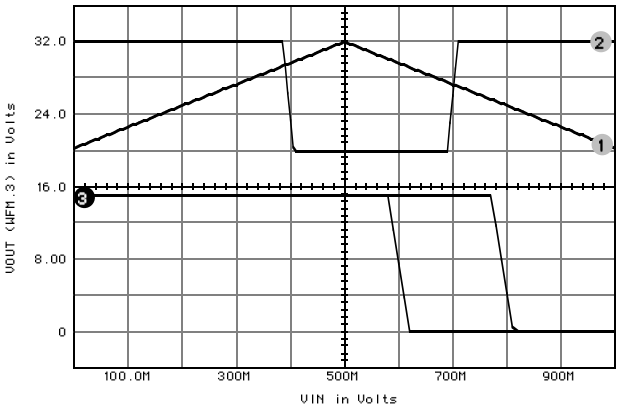


Figure 6, Simulation of the new built-in voltage controlled switch in IsSpice3. Waveforms include input ramp (1), output pulse (2) and hysteresis response (3).

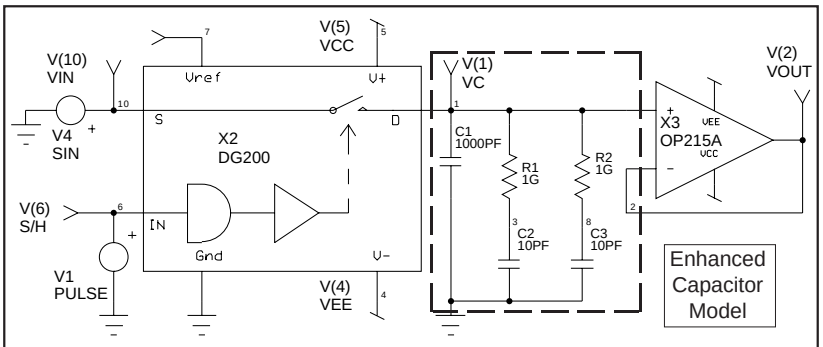


Figure 7, Schematic of a sample-and-hold amplifier. The capacitor representation includes parallel RC networks to model dielectric absorption.

Simulating A Sample-And-Hold Circuit

To study the effects of the different switch models, a simple sample-and-hold circuit was created (Figure 7). The sample-and-hold consists of an amplifier (OP215), a switch (DG200/CD4066B/Smod), and a capacitor, C1. The size of the holding capacitor is critical in sample-and-hold applications. A low value will provide fast acquisition, but will also increase the error due to the hold step and droop. While the capacitor should be as large as possible, capacitors over .1µf are not usually available in low loss dielectrics. In Figure 7, the schematic shows the equivalent circuit for a capacitor with parallel RC networks used to model the dielectric absorption.

Three simulations, each using a different switch model, were run. Run times varied from 13s for the built-in switch to 78s for the DG200. IsSpice3 simulation results, displaying the tracking of an input SIN wave for the DG200 case, are shown in Figure 8. The

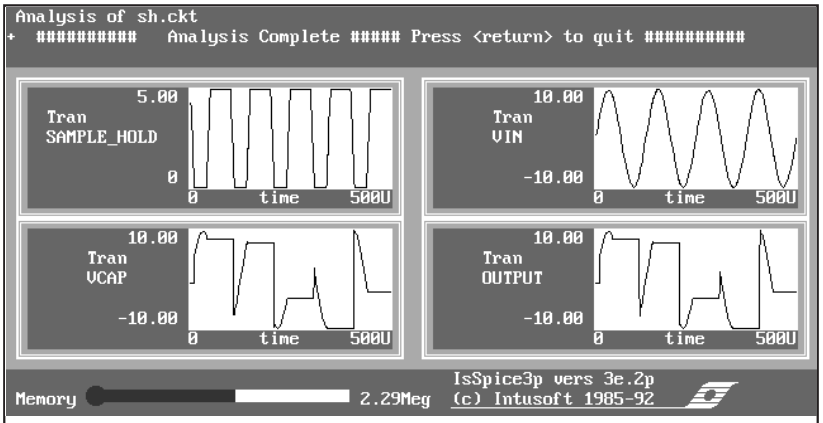


Figure 8, Output of the sample-and-hold circuit with an input sinusoidal waveform and a 10kHz sampling signal.

circuit performed well with an acquisition time of 680ns, slew rate of 20.27µV/sec, and an aperture time of 76.92ns. To study the hold capacitor effects, a simulation was run with a single capacitor and with the more complex capacitor model. The droop for the single capacitor was 87.97µV/ms. For the capacitor network, it was a more realistic 8.924mV/ms.

Conclusions

It is clear from the wealth of new modeling features in IsSpice3 that the way components are modeled is going to change dramatically over the next few years. However, even with all of the behavioral techniques available, using subcircuits containing primitive IsSpice elements to represent a component tends to produce a model that converges better and relates to the physical process. This is especially the case when higher order effects must be incorporated in a simulation. The simulation of switches is a strength of IsSpice3 due to its superior convergence with nonlinear circuit responses.

Note, Getting The Models/Schematics On Floppy: All of the schematics, circuits, and SPICE models discussed in this newsletter are available on floppy disk.

Table 1, IsSpice CMOS Analog Switch Subcircuit

```
************
.SUBCKT CD4066B 11 4   2       10  7
*Analog Switch  In Out Control Vdd Vss
X2 6 1 10 7 INVERT
M1 14 6 7 7 CD4066BN
M7 11 6 14 10 CD4066BP
M3 11 1 14 14 CD4066BN
M4 11 1 4 14 CD4066BN
M8 11 6 4 10 CD4066BP
X1 2 6 10 7 INVERT
.MODEL CD4066BN NMOS (LEVEL=1
+ VTO=3.5 KP=3.2M GAMMA=3.97U
+ PHI=.75 LAMBDA=1.87M RD=23.2
+ RS=90.1 IS=31.2F PB=.8 MJ=.46
+ CBD=63.5P CBS=76.2P CGSO=93.6N
+ CGDO=78N CGBO=128N)
.MODEL CD4066BP PMOS (LEVEL=1
+ VTO=-3.0 KP=2.4M GAMMA=3.97U
+ PHI=.75 LAMBDA=1.87M RD=21.2
+ RS=62.2 IS=31.2F PB=.8 MJ=.46
+ CBD=63.5P CBS=76.2P CGSO=93.6N
+CGDO=78N CGBO=128N)
.ENDS

********
.SUBCKT INVERT 1  2   3   4
* Inverter    In Out Vcc Vss
M1 2 1 3 3 CD49P
M2 2 1 4 4 CD49N
.MODEL CD49P PMOS (LEVEL=1
+ VTO=-2.9 KP=2M GAMMA=3.97U
+ PHI=.75 LAMBDA=1.87M RD=28.2
+ RS=45.2 IS=31.2F PB=.8 MJ=.46
+ CBD=21.2P CBS=25.4P CGSO=31.2N
+ CGDO=26N CGBO=42.8N)
.MODEL CD49N NMOS (LEVEL=1
+ VTO=2.1 KP=5M GAMMA=3.97U
+ PHI=.75 LAMBDA=1.87M RD=4.2
+ RS=4.2 IS=31.2F PB=.8 MJ=.46
+ CBD=21.2P CBS=25.4P CGSO=31.2N
+ CGDO=26N CGBO=42.8N)
.ENDS
********
```

References

[1] PMI Data Book, “Sample-And-Hold Amplifiers”, 1988

[2] Linear Technology Linear Data Book, 1990

[3] RCA CMOS Integrated Circuits Data Book, 1983

FilterMaster Professional Released

In the past, designing filters required a great deal of technical knowledge, as well as the ability and patience to work with detailed tables and text books. But today things are different. With FilterMaster Professional designers can produce results in a fraction of the time required using older methods.

The capabilities of this new program go far beyond what can be accomplished with classic filter cookbooks. FilterMaster Professional is capable of generating approximations of much greater complexity then those found in data books. But because it has been designed to guide the user, step-by-step, through the design process, even non-specialists can develop high quality minimum cost filters.

FilterMaster Professional is a PC-based program that synthesizes and analyzes passive (LC reactance) analog filters. It allows design of lowpass, highpass, bandpass, and bandstop filter circuits. Because FilterMaster Professional contains both synthesis and analysis capabilities, it allows the designer to easily optimize filter specifications and investigate the filter transfer characteristics without leaving the program.

New Features Include User Defined Response

FilterMaster Professional adds a number of impressive features, greatly surpassing the FilterMaster 1.0 version. FilterMaster 1.0 was released earlier this year and is still available. The major enhancements include: filters up to the 50th order, new user defined passband attenuation schemes, custom circuit construction, and parametric bandpass filters.

In addition to the standard filter approximations included in FilterMaster Professional: Butterworth, Chebyshev, Inverse Chebyshev, Elliptic and Bessel, there is also a choice of general amplitude approximations (maximally-flat and equal-ripple). Unlike the standard approximations, which require the same minimum attenuation for the entire stopband, these allow the user to enter arbitrary attenuation characteristics (responses with a stepped gradient, stops at specific frequencies, asymmetrical bandpasses, etc.) FilterMaster Professional can then optimize the topology and component values to match the entered specification (See Figure 9).

After the filter specifications are entered, FilterMaster Professional analyzes the filter and calculates the component values. The resulting filter structure is displayed on the screen. Several circuit editing options are available including, generation of the

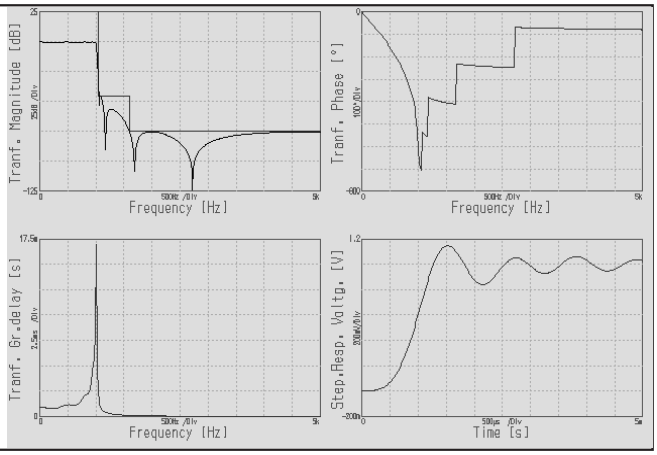


Figure 9, The new FILTERMASTER PROFESSIONAL program allows user defined tolerance schemes to be entered, as shown in the upper left graph of the filter magnitude response.

dual/reverse circuit, Norton/impedance transformation, Pi-to-Tee conversion, two-port manipulation, and direct manipulation of individual component values.

Another unique FILTERMASTER PROFESSIONAL editing option allows the designer to construct a filter component by component, with FILTERMASTER supplying the appropriate values in order to achieve the desired filter characteristics. For example, if a pole is to be specified, FILTERMASTER PROFESSIONAL will allow the designer to select from a set of series or parallel elements. Then, the program will choose the correct component values to maintain the required pole value and frequency. This allows an extra degree of freedom when constructing filters.

As shown in Figure 9, results for the transmission characteristics (amplitude, phase, group delay, and time domain pulse/step response), reflections, and impedances can all be graphed on the screen. Report quality printouts for dot matrix, laser printers, and plotters are available.

A special interface to ISSPICE and Intusoft's schematic entry program, SPICENET, allows the filters designed by FILTERMASTER PROFESSIONAL to be directly included in your circuit simulations. FILTERMASTER PROFESSIONAL also generates ISSPICE netlists with Monte Carlo component tolerances. When used with Intusoft's ICAPS package, this allows complete characterization and statistical yield analysis of your filter designs.

Availability

Upgrades from previous versions of FILTERMASTER are available. The new FILTERMASTER program will be formally debuted in November at WESCON/92 in the U.S.A., and at the Electronica convention in Germany.

Modeling Corner

The Intusoft

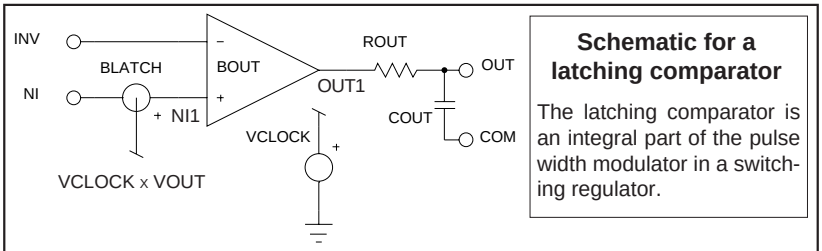
In this issue of The Modeling Corner we will introduce a model for a latching comparator using the new analog behavioral modeling capabilities in IsSpice3. The latching comparator comes from Lloyd Dixon, of Unitrode Corp. It is used in conjunction with his seminar on simulating switching regulators with SPICE. Lloyd's techniques employ a variety of new concepts. In future issues, we will explore creation of models for switching regulators in depth.

A simple comparator can be obtained with the 'B' controlled source. However, for practical use in a PWM, the comparator output swing must be limited and the output must be latched to preclude the possibility of multiple pulses in one switching period. Both problems are solved with this subcircuit.

```
.SUBCKT LATCHCOMP Inv Ni Out Com {Fs=100k}
*Rinv Inv Com 1G
BLATCH Ni1 Ni V=(V(Out,Com)-5)*V(9)
*RNi Ni1 Com 1G
BOUT Out1 Com V=100k*V(Ni1,Inv) < 0  ?  0 :
+ 100k*V(Ni1,Inv) > 5 ? 5 : 100k*V(Ni1,Inv)
* The line above reads:
+ If (100k*V(Ni1,Inv) < 0)
+       V(Out1,Com)=0
+ else if (100k*V(Ni1,Inv) > 5)
+       V(Out1,Com)=5
+ else V(Out1,Com)=100k*V(Ni1,Inv)
ROUT Out1 Out 1K
COUT Out Com {2E-6/FS}
VCLOCK 9 0 PULSE 1 0 0 .01u .01u {.02/FS} {1/FS}
*RCLOCK 9 0 1G
.ENDS
```

Note: the commented out resistors are not required in IsSpice3, but are needed for SPICE 2 versions.

As I'm sure you wondering, the If-Then-Else behavioral model can be utilized in a wide variety of applications. For example, in a switch: **B1 2 0 v=v(vctrl) < 0 ? v(3) : v(4).** Read as "If vctrl is less than 0, then v(2)=v(3), else v(2)=v(4)".



Schematic for a latching comparator

The latching comparator is an integral part of the pulse width modulator in a switching regulator.

Figure 10, Schematic showing the latching comparator. Courtesy of Lloyd Dixon, and the Unitrode course on Simulating Switching Regulators With SPICE.