Intusoft Newsletter

Personal Computer Circuit Design Tools

June 1992 Issue

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ANOTHER INTUSOFT FIRST: IGBT MODELS

SPICEMOD 2.0 is now available. The new version adds a dedicated zener model, as well as custom subcircuits for SCRs and IGBTs. SPICEMOD is the first program to be able to make SCR and IGBT models from data sheet parameters.

SPICEMOD produces models that can be used with any Berkeley SPICE compatible program. All of the models and subcircuits can be viewed and edited. A comprehensive set of test circuits is included and can be used to characterize and evaluate the models you create.

In This Issue

Custom Subcircuits

In order to model the SCR and IGBT devices, two newly designed subcircuits have been included in SPICEMOD. The SCR was described in the Feb. 92 issue, while the IGBT subcircuit is briefly described on page 25-12. Other additions include improvements in the DC characteristics for small signal and power Mosfet models and better calculation of the BJT capacitance and transit time parameters. The on-line help system has also been augmented with more information on how the data sheet parameters relate to the SPICE model and subcircuit parameters.

Ordering and Technical Information

SPICEMOD 2.0 is available now. Registered owners of version 1.x can update for the difference in price.

SPICEMOD Models All Types of Semiconductors

- **Diodes** - Silicon, GaAs, Ge, PN, Schottky, Bridge, Computer, Switching, Rectifier
- **Zeners** - All Ratings
- **BJTs** - Silicon, Germanium, NPN/PNP, Low/Medium Power, Amplifier, Signal
- **Power BJTs** - Silicon, Germanium, NPN/PNP, High Power
- **Darlington BJTs** - NPN/PNP, Signal, Power
- **JFETs** - N/P Channel, Enhancement/Depletion, Amplifier, Small Signal
- **MOSFETs** - NMOS/PMOS, Enhancement/Depletion, Amplifier, Small Signal
- **Power MOSFETS** - NMOS/PMOS, Enhancement/Depletion
- **SCRs** - SCRs, GTOs, Low and High Power, Sensitive Gate
- **IGBTs** - N/P Channel

Solid State Relays and Switches

The solid-state relay (SSR) has found use as a replacement for the electro-mechanical relay in communications, industrial control, and instrumentation applications. While not completely supplanting the mechanical variety, the SSR has a number of advantages that make its use preferable (Table 1) [1].

Advantages	Disadvantages
Longer lifetime	Expensive
Faster speed	Nominal voltage drop
Minimal maintenance	Produces heat
Immune to shock	Leakage current
Logic compatible	Fewer switching functions
Few EMI/RFI problems	
No contact bounce	
Simpler design	
High reliability	
Small size	

Table 1, Advantages and disadvantages of SSRs as compared to electro-mechanical relays.

A quick glance at recent articles on SSRs provides an indication of their growing variety and capability [2,3]. Orders of magnitude improvement over electro-mechanical relays in power, size, reliability, and efficiency make the SSR a superior choice for many applications. In addition, the SSRs ability to switch both resistive and inductive loads over a wide range of levels has improved as new semiconductor combinations have been constructed. Table 2 lists several types of SSRs and their characteristics [1,4].

Due to the nonlinearities generated in switching circuits, SPICE simulation of SSRs is both desirable and profitable. In part 1 of this article we will discuss models for a simple analog behavioral switch, a CMOS analog switch, and for an optocoupled SCR.

A Generic Switch Model

Although a model for an electro-mechanical relay can be built [5], a more efficient model of a switch is available in IsSpice. For those

Table 2, Characteristics of Various Relays and Switches

	Optocoupler	PhotoMos	OptoSCR	Analog Switch
Contact resistance (Ω)	10	5	4	50
Isolation resistance (GΩ)	100	10	100	.01
Volume (cm^3)	.25	.22	.25	.2
Current range (A)	10µ-40m	0-.7	8m-5	10µ-25m
Voltage range (V)	1-30	0-400	1-600	0-18
Max. continuous current (A)	.2	.7	.3	.025
Pick-up time (µs)	1	100	50	.2
Pick-up power* (mW)	12	3	35	.01
Power consumption (mW)	60	100	100	125

*@ 20°C and max. continuous current. Contact type for all devices is normally open.

who are looking for a simple way to switch between two different impedances, the Intusoft analog behavioral switch model is the best solution [6]. The switch is created using the IsSpice dependent voltage controlled current source (G1) tied back onto itself. Because the switch uses only two elements it simulates very quickly. Its impedance can be controlled over time allowing it to replace mechanical or semiconductor switches and emulate switch bounce and variable on resistances.

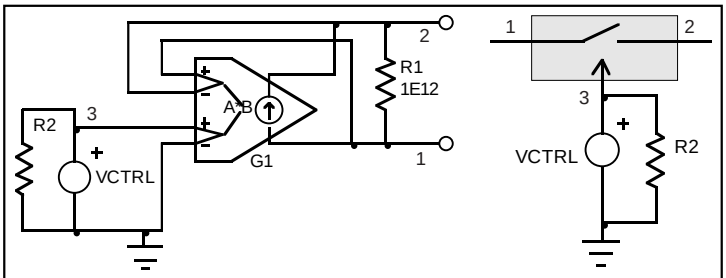


Figure 1, Generic switch configuration (left) and switch symbol (right in the shaded area). An extra resistor, R2, is needed around the controlling voltage source in order to provide a DC path to ground.

The generic switch is very easy to use. Applying zero volts to the control input opens the switch. The open resistance used here is R1=1E12Ω. The open resistance value should be made just high enough to appear as an infinite impedance relative to adjacent circuitry. Applying any voltage to the control input, node 3, closes the switch with a resistance equal to 1/V(3). For example, applying a voltage pulse, 0 to 1 volt, to the control input will change the resistance seen from port 1 to port 2 from 1E12Ω to 1Ω.

Important Note: If you apply a voltage to the control input using a voltage source, you will have to place a resistor across the voltage source in order to have a DC path to ground; a SPICE requirement. The problem occurs because the input to a voltage controlled source appears as an infinite impedance. This allows the dependent source to sample a node voltage without loading the circuit. Connecting a large resistor (R2 as shown above) to the source will fix the problem without affecting circuit operation.

Creating An Analog Switch

Use of an analog switch, such as the Siliconix DG200, is popular due to its easy logic interfacing. Since macro modeling techniques could not be used to simplify the switch structure, the actual IC topology was duplicated as described in the data sheet. This approach is a distinct contrast to the behavioral switch. However, it will enable most higher order effects to be simulated if the proper models can be ascertained. Little data sheet information is available on the actual internal Mosfet devices and models are not available from the vendor. Therefore, SpiceMod, the SPICE

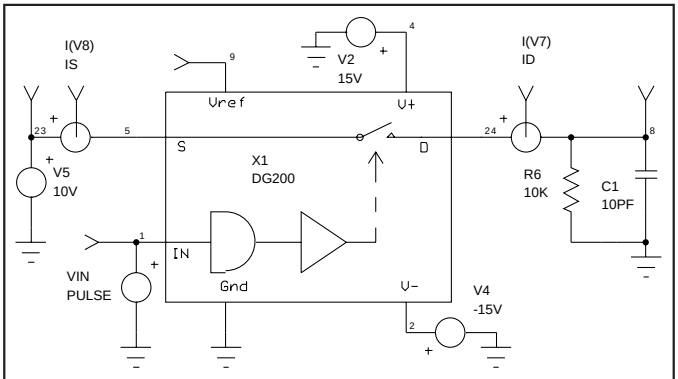


Figure 2, Test circuit for the DG200 CMOS analog switch (Siliconix). Setup shown is for the measurement of the delay, rise, fall, and switching transients.

modeling program, was used to make the CMOS models. As in the case of the Dual-Gate Mosfet [7], SPICEMOD was able to make accurate estimates for PMOS and NMOS devices even though scant information was available.

After some initial testing, the KP and capacitance parameters of the individual N and P channel devices were tweaked. Unfortunately, the device widths were not known so estimations based on trial simulations were used. Very accurate responses for the on-resistance, leakage currents, switching times, and off isolation were obtained. Figure 2 shows one of the test circuit variations. The results are shown in Figures 3 and 4. Although the subcircuit contains 18 Mosfets, it still simulates very quickly on ISSPICE. The ISSPICE subcircuit netlist is given in Table 3.

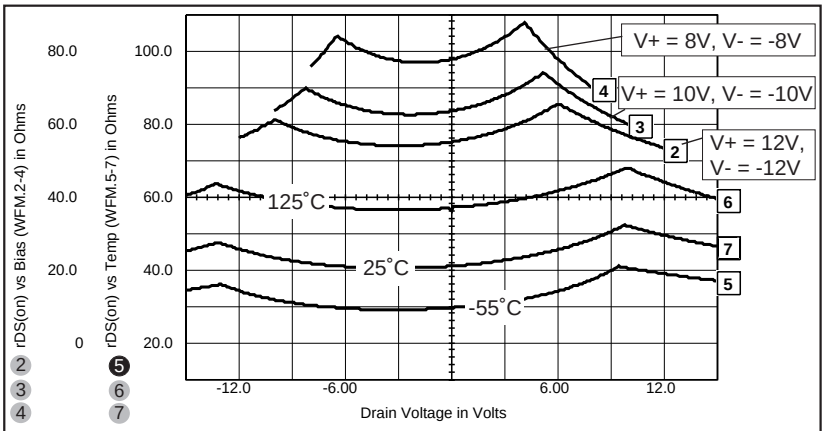


Figure 3, Waveforms 2, 3 and 4 are from simulations at 25˚C. Waveforms 5, 6, and 7 are from simulations at V+=15V and V-=-15V.

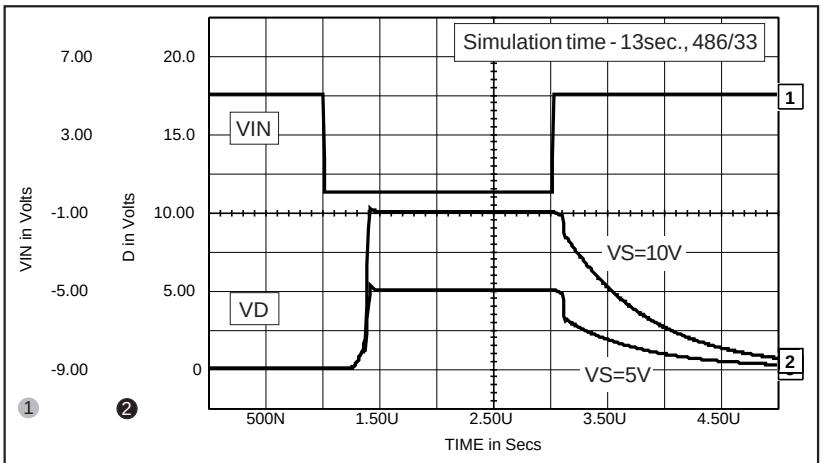


Figure 4, Transient simulation results of the DG200 switching tests.

Combining An SCR With An Optocoupler

BJTs, JFETs, Thyristors, Mosfets, and Triacs can be used as relays to switch DC or AC circuits via the application of a low level pulse. However, since these elements offer inadequate separation between the control and load circuits, an additional barrier, such as an optocoupler, is needed.

Optocoupled SSRs are constructed using GaAlAs LEDs that are optically coupled to the semiconductor device. The basic modeling concepts for optoisolators are discussed in Ref. 6. In the case of the optoSCR, the output transistor of the optoisolator is replaced with an SCR that is modeled by the new SPICEMOD program. The input to the LED then controls the SCR triggering. As shown in Figure 5, the SCR will conduct until the following negative zero crossing as long as the control signal is present.

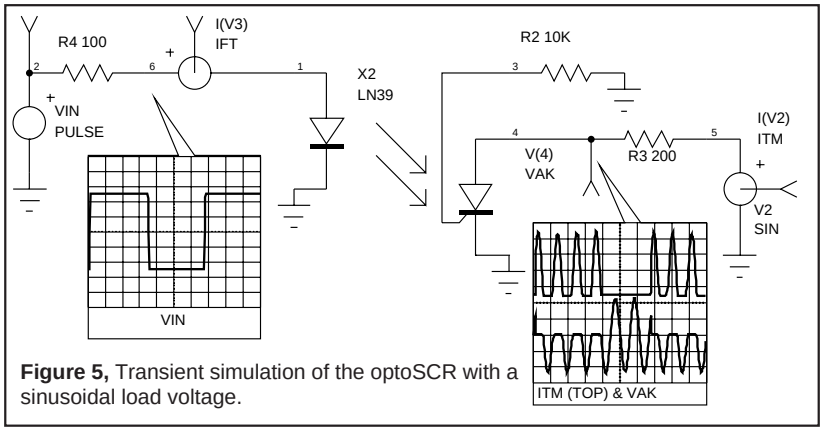


Figure 5, Transient simulation of the optoSCR with a sinusoidal load voltage.

Conclusions

All of the schematics, test circuits, and SPICE models discussed in this article are available on floppy disk. Additionally, models for the 4N40 and the DG201 are included. In Part 2 of this article we will simulate several opto-coupled devices including PhotoMOS and Optotriac relays. We will also look at the CD4066 CMOS analog switch and demonstrate some sample and hold circuits.

Table 3, IsSpice Analog Switch and OptoSCR Subcircuits

```
.SUBCKT DG200 6  10  17 7  3    15 18
*Connections  In Gnd S  D  Vref V- V+  Siliconix DG200
M1 6 8 21 21 NMOS W=55U
M2 12 21 9 9 NMOS W=55U
M3 5 4 9 9 NMOS W=55U
M4 9 14 15 15 NMOS W=55U
R1 14 10 5K
R2 10 3 23K
R3 4 3 5K
R4 8 18 5K
R5 18 3 220K
M5 12 5 18 18 PMOS W=55U
M6 5 5 18 18 PMOS W=55U
M7 2 12 6 10 NMOS W=55U
M8 2 12 18 18 PMOS W=55U
M9 20 2 16 15 NMOS W=55U
M10 20 2 18 18 PMOS W=55U
M11 16 2 18 18 PMOS W=55U
M12 16 2 15 15 NMOS W=55U
M13 19 20 18 18 PMOS W=55U
M14 19 20 15 15 NMOS W=55U
M15 7 20 17 11 NMOS
M16 17 19 7 18 PMOS
M17 17 20 11 11 NMOS
M18 11 19 15 15 NMOS
.MODEL NMOS NMOS (LEVEL=1 VTO=1 KP=1.4M
+GAMMA=.124 PHI=.75 LAMBDA=2.49M RD=13.5
+RS=2.5 IS=10F PB=.8 MJ=.46 CBD=63.6P
+CBS=76.3P CGSO=84.2N CGDO=70.2N
+CGBO=115N)
.MODEL PMOS PMOS (LEVEL=1 VTO=-1 KP=1.4M
+GAMMA=.124 PHI=.75 LAMBDA=2.49M RD=17.1
+RS=4.1 IS=10F PB=.8 MJ=.46 CBD=85.9P
+CBS=103P CGSO=113N CGDO=94.8N CGBO=156N)
.ENDS
```

```
.SUBCKT LN39  17   18  1  3  2
*Connections  LA   LC  A  K  G - Motorola 4N39
QP  6 4 1  POUT OFF
QN  4 6 5  NOUT OFF
RF  6 4    10.6MEG
RR  1 4    7.11MEG
RGK 6 5    5.62K
RG  2 6    92.3
RK  3 5    .233
DF  6 4    ZF
DR  1 4    ZR
DGK 6 5    ZGK
H1 2 3 VLED -.8 93.3
VLED 17 16
D1 16 18 DLED
.MODEL ZF D (IS=.12F IBV=3.75U BV=200
+ RS=1.6MEG)
.MODEL ZR D (IS=.12F IBV=3.75U BV=266)
.MODEL ZGK D (IS=.12F IBV=3.75U BV=6)
.MODEL POUT PNP (IS=120F BF=1 CJE=1.34P)
.MODEL NOUT NPN (IS=120F BF=100 RC=.933
+ CJE=1.34P CJC=286F TF=18.95U TR=1.27M)
.MODEL DLED D (IS=140P RS=520M N=2.63 BV=6
+ IBV=10U CJO=50P VJ=.75 M=.333 TT=432N)
.ENDS
```

References

[1] The Modern Relay, Dr.-Ing. J. Eichmerier, SDS-Relais AG, 1988.

[2] “Solid-state relays meet requirements and handle demanding applications”, T. Ormond, , EDN Magazine, March 16, 1992.

[3] “Explaining microelectronic relays”, D.J. Butchers, International Rectifier, Components in Electronics Magazine, March 1992.

[4] Microelectronic Relay Designer's Guide, International Rectifier, 1990.

[5] Analog Computation, Jackson, McGraw-Hill, 1960

[6] PreSpice User's Guide, Intusoft, 1988.

[7] “Modeling Dual-Gate Mosfets”, Intusoft Newsletter, August 1991

Simulating Class C RF Amplifiers

IsSpice can be a versatile tool for RF work as long a few simple precautions are taken. Significant parasitics must be included in the circuit description, models of active devices must be represented using subcircuits, and selection of transient analysis options must be considered. The transient options include the total analysis time, the data printout step and delay, and the simulator error tolerances. Of course, IsSpice will also do AC analyses of RF circuits, but this is not its strong suite as many other simulators will also do linear small signal work. The real strength of IsSpice is in its time domain capability where either repetitive or non-repetitive waveforms can be used as stimulus. This ability is handy for burst work, measurement of peak stresses under normal operation or momentary fault conditions, detailed study of bypass networks, and many other conditions. Since test points do not load the circuit in any way, measurements that would be impossible on the bench can be easily made with the IsSpice simulation.

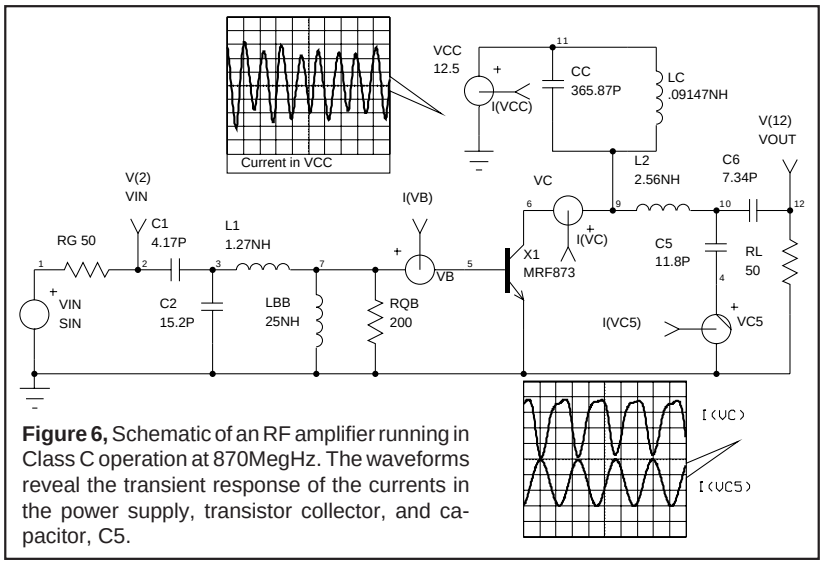


Figure 6, Schematic of an RF amplifier running in Class C operation at 870MegHz. The waveforms reveal the transient response of the currents in the power supply, transistor collector, and capacitor, C5.

Shown in Figure 6 is a typical circuit used to simulate the operation of a class C power device. The device used here, X1, is the Motorola MRF873 NPN power BJT. It can produce 15 watts of output power in the 806-960 megahertz range. RG provides 50Ω impedance for the generator. C1, C2, and L1 are used for input matching. LBB and RQB are for DC return to ground and Q limiting for the base. L2, C5, and C6 are used for output matching. CC and LC form a return to VCC for the

collector. RL is 50Ω. The generators VB, VC, and VC5 are zero valued sources used to measure the instantaneous circuit currents.

A typical simulation of Figure 6 requires 25.6 seconds on a 486/33 (RELTOL=.0003). The change in RELTOL was required for increased accuracy, although the default of .001 provided comparable results. At 870 megahertz one cycle takes about 1.1ns. Since class C circuits need some number of cycles to stabilize, this circuit was simulated from T = 0ns to T = 20ns with output data accumulated from 15ns to 20ns. The simulation has about 15 cycles to settle before data is gathered and is pretty well settled by that time.

After initial testing of a nominal case (VCC=12.5, Power In=3W) the parameter sweeping features of the ICAPS program were used to sweep the input power. The input power is controlled by the voltage of VIN. In order to easily control the simulation parameters, a simple subcircuit was made to convert input power in watts to the peak voltage required by the IsSpice voltage source. The power supply, VCC, was also made a variable. The conversion is shown below.

Replace:	**With:**
VCC 11 0 12.5	VCC 11 0 VTEMP
VIN 1 0 SIN 0 Vpeak 870 .5N	X2 1 0 VSIN {PIN=PTEMP}
	.SUBCKT VSIN 1 2
	VIN 1 2 SIN 0 {(PIN∗50)^.5∗2∗2^.5} 870 .5N
	.ENDS

After setting up the extended syntax, the control statements

```
∗OPT VTEMP=5 TO 17 STEP=.25        and
∗OPT PTEMP=.5 TO 6 STEP=.25
```

can then be used to sweep the parameters VTEMP (equal to the power supply voltage) and PTEMP (input power in watts).

During the simulation the waveforms at various points were sampled. IntuScope was used to reduce the IsSpice voltage and current data into output power and DC power values. After the sweep, IntuScope then calculated the power gain (10∗lgt(Pout/Pin)), efficiency (Pout/Pdc), and dissipation (Pout-Pdc). Since there is no circuit loading associated with monitoring voltage and current, measurement of the capacitor RMS current and peak voltage is possible. For nominal power input, the peak-peak voltage across C5 was 93.00V, while the RMS current was 2.082A. This type of data is vital for making informed component selection decisions.

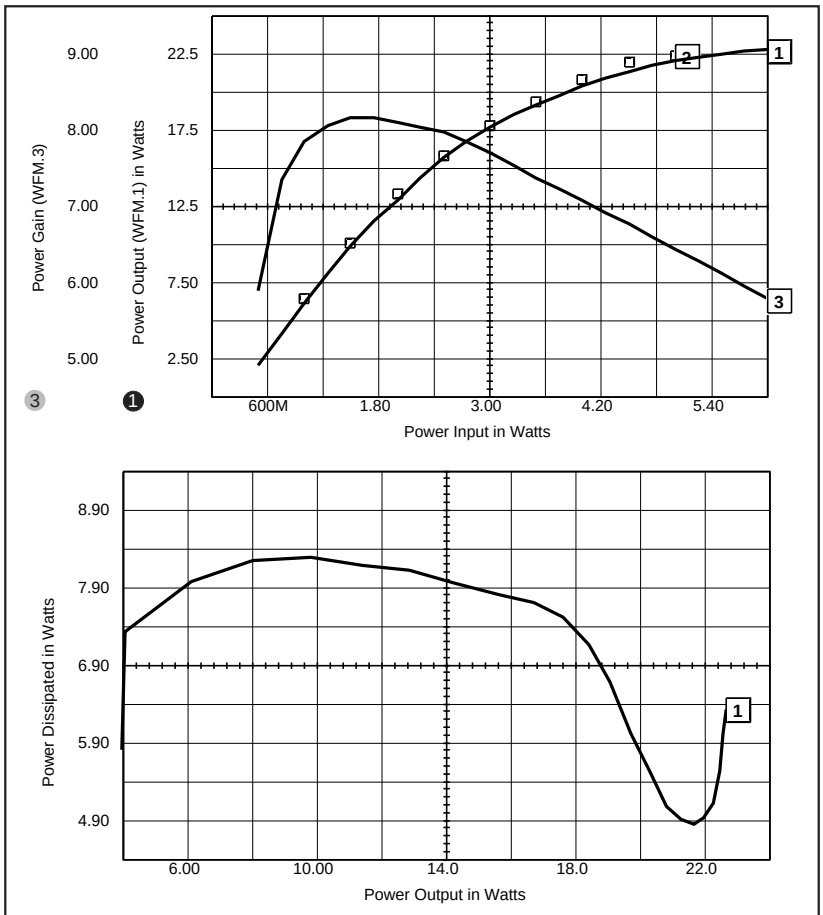


Figure 7, Power output, power gain, and power dissipation results from the IsSpice analysis of a class C amplifier (870MegHz, VCC=12.5V). The square boxes (above) show the data sheet response for power output.

Figure 7 (top graph) shows the excellent tracking between the IsSpice simulation and the data sheet values for output power and power gain vs. input power. The lower graph contains the results for the power dissipation in the MRF873. Figure 8 shows the simulation results for efficiency and output power vs. VCC at constant input power.

Once the relationships were studied and a final output power and VCC range were selected for detailed analysis, the physically impractical and somewhat narrow bandwidth lumped element networks in Figure 6 were replaced with transmission lines. The t-line values were calculated to match published input and output impedances. Other values were taken from the Motorola data sheet. The simulation time became 5 to 10

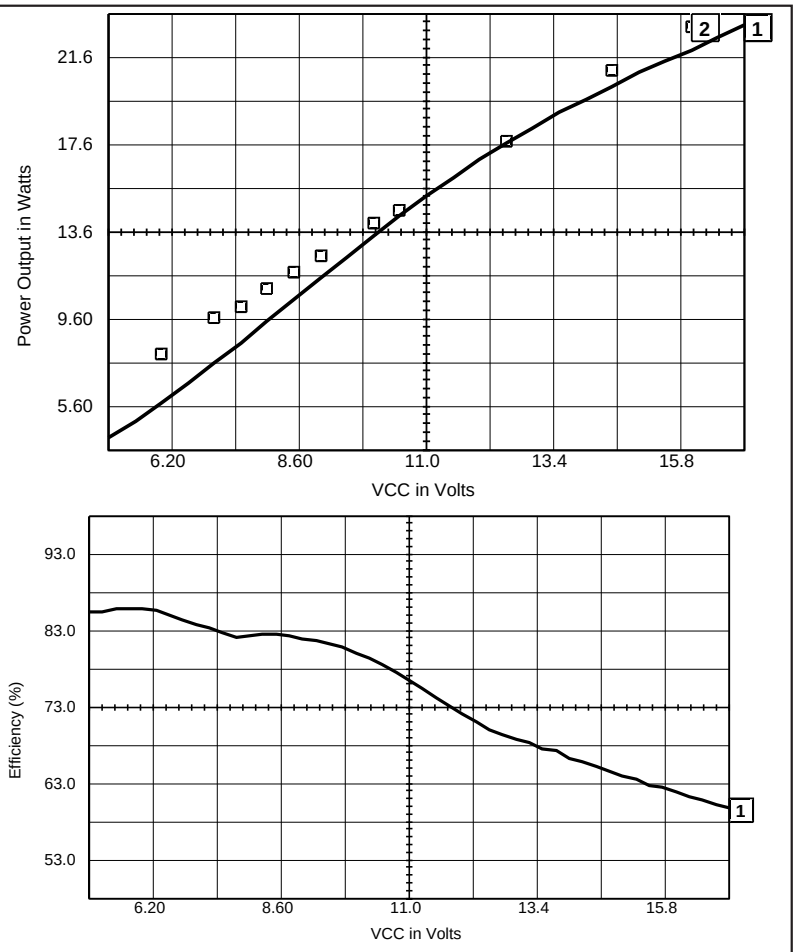


Figure 8, Power output and amplifier efficiency vs. VCC. Square boxes indicate the data sheet response for power output.

```
.SUBCKT MRF873 1 2 3
LC 1 4 0.50E-9
LB 2 6 0.60E-9
LE 5 3 0.07E-9
CC 4 3 15.0E-12
CB 4 6 1.00E-12
Q1 4 6 5 QR01
.MODEL QR01 NPN (BF=98 VAF=150 VAR=10.0 RC=.15 RB=1.43 RE=.26
+ IKF=1.0 ISE=7.6E-14 TF=1.2E-11 TR=1.7E-09 ITF=1.7 VTF=5.3
+ CJC=10.7E-12 CJE=12E-12 XTI=3.0 NE=1.5 ISC=2.4E-14 EG=1.11
+ XTB=1.5 BR=2.29 IS=8E-15 MJC=0.33 MJE=0.33 XTF=4.0 IKR=0.5
+ KF=1E-15 NC=1.7 RBM=1.02 IRB=1.60E-02 XCJC=0.5)
.ENDS
```

Table 4, The IsSpice subcircuit netlist for the MRF873 RF power transistor. Connections are Collector(1), Base(2), Emitter(3). The subcircuit may be used with any SPICE simulator.

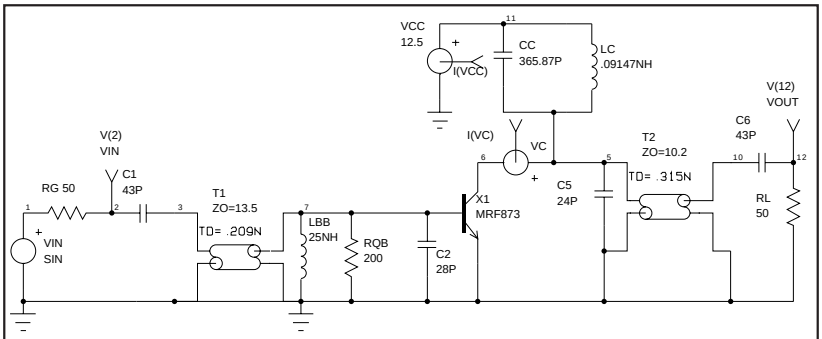


Figure 8, In order to provide a more realistic simulation, the physically impractical lumped elements are replaced with transmission lines. The transmission line values are calculated to match published input and output impedances.

times longer with the transmission lines but was still reasonable at 3 to 4 minutes per run. The simulation results were within 10% of the lumped element approach. Based on the increased run time and comparable results achieved, it is advisable to use the lumped element approach for the majority of the simulations, saving the transmission line models for the final simulations. The complete set of simulations is available on floppy disk.

From the accurate results presented here, it is clear that simulation of class C RF circuits is practical and productive as long as the circuit and transistors are modeled properly.

Note: Thanks to Bill Sands of **Analog & RF Models**, specialists in the creation of RF device models for his substantial contributions to this article.

EDN Article Reviews SPICE Simulations

For those who are looking for a comparison of different SPICE programs, check out the May 21, 1992 issue of EDN Magazine. In the article entitled **"DOS Based SPICE Software"**, EDN editor Ann Swager reviews how eight different CAE tool vendors simulated four complex circuit designs. **Of the eight vendors who participated, Intusoft was the only vendor of SPICE software that completed all circuit simulations.** Of note: Microsim, makers of Pspice, only performed one simulation. We congratulate the Intusoft Technical Support staff on an excellent job.

The article contains some very interesting insights into the problems encountered in simulation and the different approaches taken to solve them. In upcoming newsletters, Intusoft will be thoroughly reviewing each circuit and presenting detailed results.

P.S. Check out the photo on the title page of the article.

Modeling Corner

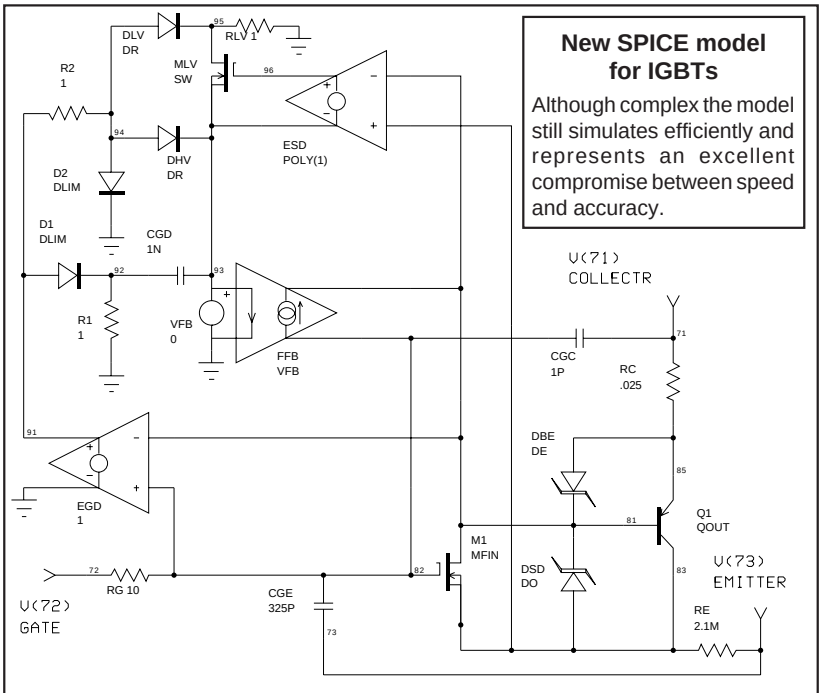
The Intusoft

In this issue of The Modeling Corner we will briefly introduce a new SPICE model for IGBTs. An in-depth description of the subcircuit and how models for specific IGBT devices can be created from data sheet parameters will appear in a future newsletter.

This is the first IGBT model ever available in a form that can be used for a variety of IGBTs and for virtually all SPICE versions. The model is generic in nature, meaning, that component values in the subcircuit can be easily recalculated to emulate different IGBT devices. The new model accurately simulates:

- Switching loses
- On-voltage
- Turn-on/turn-off delay
- Active output impedance
- Nonlinear capacitance effects
- Forward/reverse breakdown
- Rise time and tail
- Collector family curves including mobility modulation

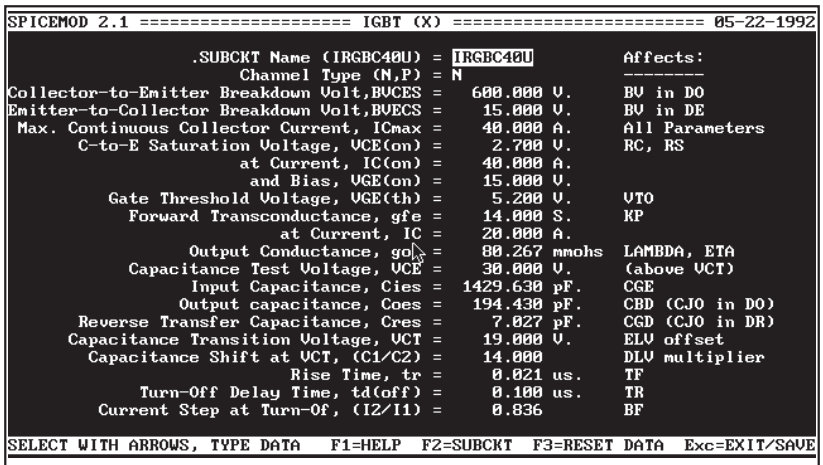
For those who are interested in obtaining IGBT models, there are several possible opportunities. First, *Intusoft Newsletter*



New SPICE model for IGBTs

Although complex the model still simulates efficiently and represents an excellent compromise between speed and accuracy.

Figure 8, Schematic showing the subcircuit topology of the IGBT SPICE model. The subcircuit is implemented in the new version of SPICEMOD.




```
.SUBCKT IRGBC40U 71 72 73
*     TERMINALS:  C  G  E
* 600 Volt  40 Amp  21NS
* N-Channel IGBT
Q1  83 81 85     QOUT
M1  81 82 83 83  MFIN L=1U W=1U
RC  85 71  21.1M
RE  83 73  2.11M
RG  72 82  25.6
CGE 82 73  1.42N
CGC 82 71  1P
EGD 91  0 82 81  1
VFB 93  0  0
FFB 82 81  VFB  1
CGD 92 93  1.41N
R1  92  0  1
D1  91 92  DLIM
DHV 94 93  DR
R2  91 94  1
D2  94  0  DLIM
DLV 94 95  DR 13
RLV 95  0  1
ESD 96 93  POLY(1) 83 81  19  1
MLV 95 96 93 93  SW
DSD 83 81  DO
DBE 85 81  DE
.MODEL QOUT PNP (IS=377F NF=1.2
+BF=5.1 CJE=3.48N TF=6.04N)
.MODEL MFIN NMOS (LEVEL=3
+ VMAX=400K THETA=46.1M ETA=2M
+ VTO=5.2 KP=2.12)
.MODEL SW NMOS (LEVEL=3 VTO=0
+ KP=5)
.MODEL DR D (IS=3.77F CJO=100P
+ VJ=1 M=.82)
.MODEL DO D (IS=3.77F BV=600
+ CJO=2.07N VJ=1 M=.7)
.MODEL DE D (IS=3.77F BV=14.3
+ N=2)
.MODEL DLIM D (IS=100U)
.ENDS
```

Figure 9, The SpiceMod 2.0 input screen (top) shows the extensive list of IGBT data sheet parameters that can be entered. The resulting subcircuit, of the International Rectifier IRGBC40U IGBT, is shown above.

subscribers will receive the enclosed model along with several other models on the newsletter floppy disk. Second, a library of 65 IGBT models is included in the PreSpice version 3.0 package. And third, registered owners of Intusoft software can avail themselves of Intusoft's free modeling services.

At this time, several manufacturers, including International Rectifier, are preparing to release IGBT models created with SpiceMod 2.0. Contact the manufacturer of your IGBT devices for more information. The IGBT model, like all of Intusoft's models, will work on any SPICE program on any platform.