



(310) 833-0710

*Personal Computer
Circuit Design
Tools*

NEWSLETTER

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PRE_SPICE UPDATE TO SHIP APRIL 30, 1987: A major PRE_SPICE update shown at ELECTRO/87 earlier this month is set to ship. An optimizer and an interactive circuit analysis program selector, ICAPS have been added. The component library has been extended to include Switched Capacitor Network models, digital circuit Macro Models and a family of system design elements. The old library and programs have been updated along with the documentation. More on what the new programs can do after a few news items.

******* Money Back Guarantee *******

We have been shipping our software with a 30 day money back guarantee since last August. The guarantee policy simply requires that if for any reason you are unsatisfied with the product(s) that you return the software along with our form stating that you have read and agree to the license and have destroyed all software and documentation copies. We do exclude developers of similar products and their agents. We began advertising this new policy in January and have extended it to foreign sales.

******* No Copy Protection *******

Our distribution diskettes have never been copy protected. Intu_Scope version 1.2 had a feature preventing it from being copied from or moved around in a hard disk. Even this feature has been removed from version 2.0.

These policies are in place to make it easier for you to buy and use our products. Our price structure is the lowest in the industry, and to keep the prices down we rely on your cooperation in preventing unlicensed distribution.

***** Oops ! * ****

Sorry about misspelling OrCAD's name in the last newsletter.

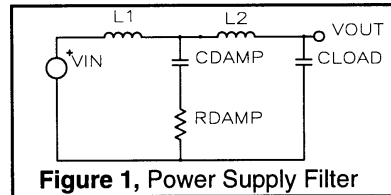
In the November newsletter we reversed the polarity of the voltage controlled voltage source on page 3-11. The source description should be changed to "E 2 3 1 2 ..." and the input and output polarities reversed in the figure.

***** An Optimizer Example *****

The optimizer was designed to allow IS_SPICE parameter values to be varied automatically. Families of output data can be plotted or the best value for a particular component or parameter can be found.

The example shown here is for a power supply input filter. The topology shown in figure 1 is a commonly used standard. The capacitor, CLOAD,

filters the pulsating current caused by a switched mode converter. Its value is based on its ripple current carrying ability, cost, size and the permissible voltage ripple at its terminals. The remainder of the filter is used to



bring the input ripple current to within acceptable limits. The filter circuit will have some frequency domain peaking, causing the switched mode regulator to experience greater stress. The circuit designer needs to choose values for both RDAMP and CDAMP to minimize ripple, cost and size.

Two analyses were run to show how the peaking and values of RDAMP and CDAMP relate. The first run used the sweeping features to vary RDAMP from 2 to 20 Ohms in one Ohm steps for a family of CDAMP capacitors from 5UF to 70UF in 5UF steps. Damping was chosen as the objective function. Damping was measured using Intu_Scope by taking the reciprocal of the maximum value of the transfer function.

The second run was made to find the optimum value of RDAMP for each CDAMP, and is shown in the jagged curve through the curve family in figure 2. Armed with this information, the designer can now pick the capacitor and resistor from these curves that are best suited to the cost and size constraints.

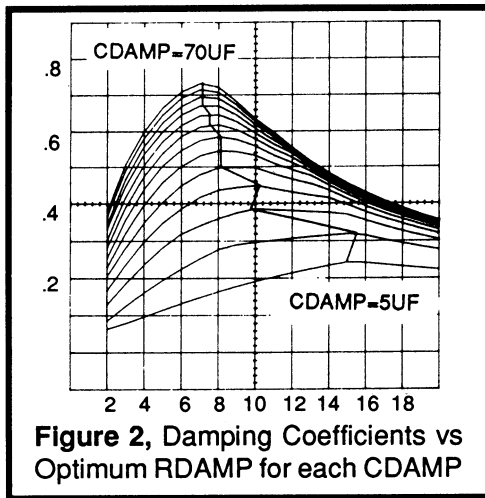


Figure 2, Damping Coefficients vs Optimum RDAMP for each CDAMP

This is a fairly simple example of what can be done with the optimizer. You could probably solve the differential equations or look up the design parameters in a handbook, however, adding a few more circuit elements would make such an approach impossible. Pulse width modulator and op-amp models available in PRE_SPICE could be included in a more complete power supply model to further refine these computations.

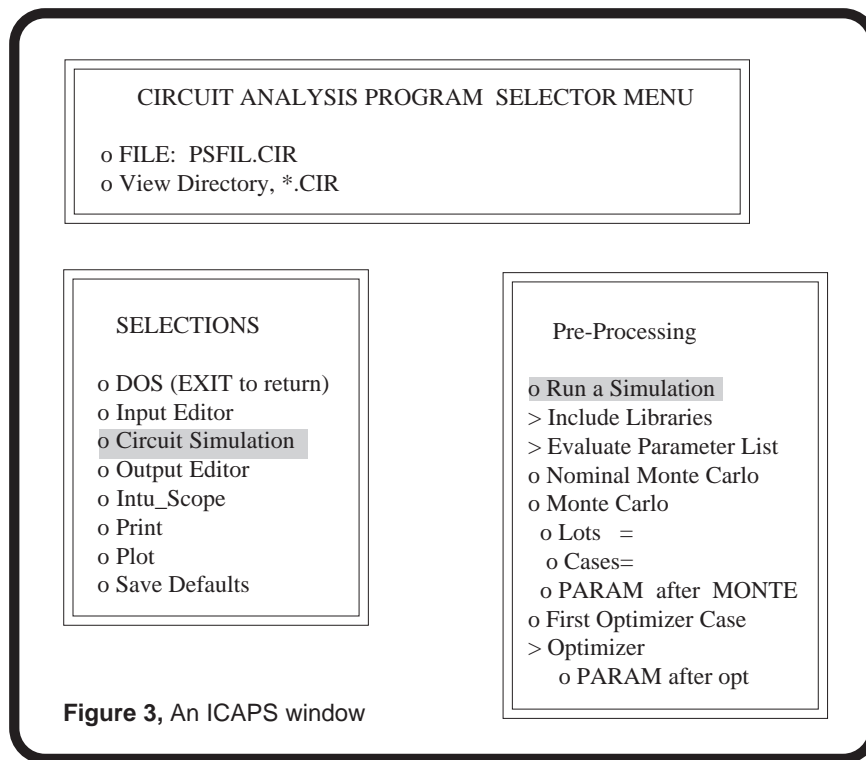


Figure 3, An ICAPS window

**** ICAPS makes life easy ****

The screen shown in figure 3 illustrates the ICAPS window used for the optimizer analysis. Menu items are turned on and off using the keypad

arrows. The correct program sequence and command line options are selected automatically. The right hand menu changes to reflect the topic selected. Total analysis control is accomplished using ICAPS, making it easy to learn and use the suite of Intusoft circuit simulation programs

****** Model Summary ******

The following model libraries and their contents are now available in PRE_SPICE version 2.0. The generic models allow you to make simple data sheet entries to get working static and dynamic models, for example, the generic transistor only needs Cob, Ft, Ts, and ICmax to get your circuits running. The more detailed models and descriptions in the documentation can be used as templates when more accuracy is needed.

DEVICE.LIB

Diodes	PNP Transistors	Opto-Isolator
Generic	Generic	4N25
Zener	2N2907	Comparator
1N4001	2N3906	LM111
1N4148	NPN Power	Power Electronics
1N5811	Generic	Transformer
1N5816	2N3055	Saturable Core
1N3909	2N6277	Pulse Width Modulator
NPN Transistors	Power FET	Misc.
Generic	IRF150	GaAs FET
2N2222	SCR	
2N3904	2N6397	
2N3507		

NONLIN.LIB

Bipolar Op-Amp
 FET Op-Amp
 UA741
 LF156
 OP27

LIN.LIB

Bipolar Op-Amp
 FET Op-Amp
 UA741
 LF156
 OP27

SYS.LIB

Integrator
 Differentiator
 2,3 Input Summer
 Multiplier
 lead-lag
 Servo

SCN.LIB

Floating Capacitor
Positive Storiator
Negative Storiator
Unit Time Delay
Zero Order Hold
C-resistor
SCN Integrator
Toggle Switch
Switch

DIGITAL.LIB

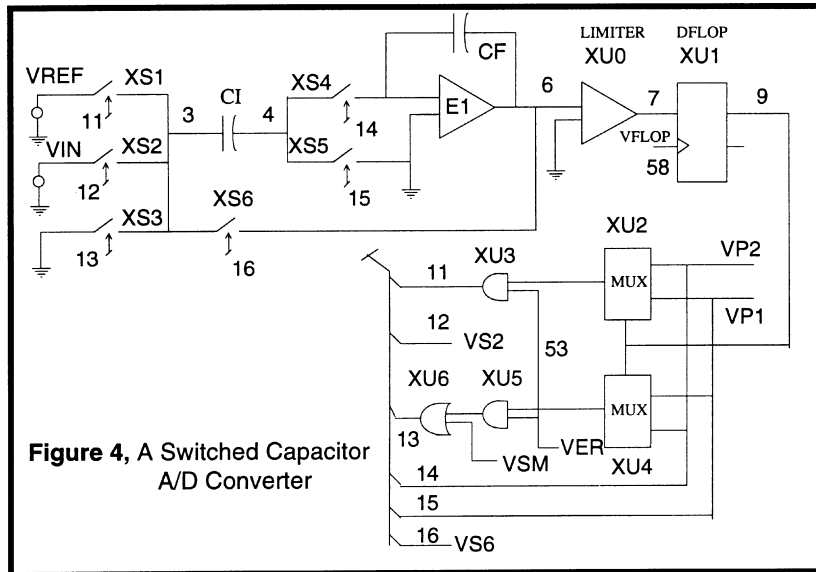
2,3 input NAND
2,3 input AND
2,3 input NOR
2,3 input OR
D Flip Flop
Shift register stage
Exclusive OR
Inclusive OR
Inverter
1 bit A/D (analog interface)

******* APPLICATION NOTE *******

Continuing from the February newsletter focus on Switched Capacitor Networks, an SCN A/D converter will be simulated. The A/D converter requires mixed mode, analog and digital, models. We will describe a set of higher level models for each of the A/D elements that allows a system level simulation. Motivating this approach, is the need to understand circuit operation at the system level, followed by detailed examination of each of the circuit blocks. Once an overall model is running, then the various blocks can be examined one at a time to see how they work in the design.

The schematic of figure 4 and PRE_SPICE listing in table 1 shows the A/D topology we will study. This is a reflex A/D converter, that is, the conversion is repeated successively using the same set a components in a recursive fashion. The SCN integrator is first used to sample the input voltage. If the output is positive, the reference is subtracted, otherwise it is added. The resulting voltage at the integrator output is the error after each conversion. Rather than dividing the reference by 2, the usual case for successive approximation, the error is multiplied by 2. This approach reduces the contribution of amplifier errors for the lower order bits. The comparator and D Flip Flop are used to quantize the output and control the switching operation.

Reference 1 describes some of the basics of this type of conversion while reference 2 shows how a capacitor ratio insensitive feature can be added. Other features can be added to remove integrator and comparator offset errors. SCN conversion techniques have been reported with accuracy on the order of 12 bits. The design shown here should achieve 6 to 8 bits accuracy and is suitable for many audio signal processing applications.



Key items to be designed are:

1. Integrating Amplifier
2. Comparator

Important circuit parasitics are:

1. Clock feedthru, integrator, comparator and switch
2. Switch resistance
3. Amplifier and Comparator offsets

Not shown in the schematic is the means to initialize the integrating capacitor to zero, since this condition is initialized in the simulation. The following Elements Models are needed for the system level simulation:

1. Switch
2. Amplifier
3. Comparator
4. D Flip Flop
5. Logic Gates and multiplexer

Clocks, Capacitors and Sources use standard IS_SPICE built in elements. Switches and Logic macro's have been described in previous newsletters and are reproduced here without detailed explanation. Table 2 shows the library listings for these elements. Logic elements use

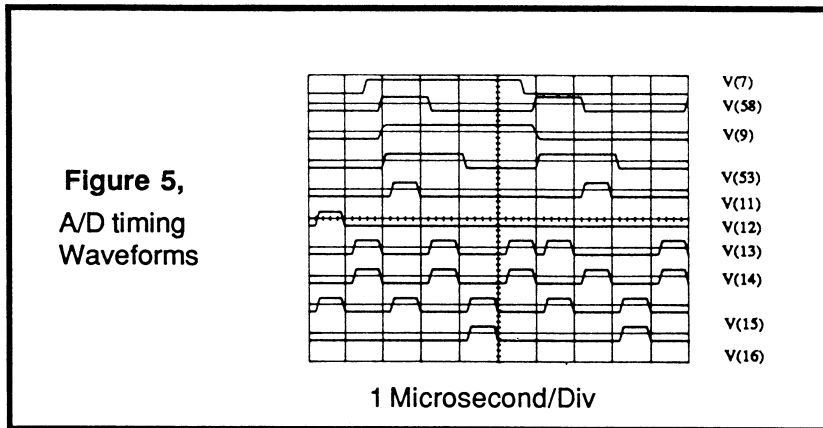
the threshold logic macro's described in the November 1986 newsletter and the switch is as described in the April 1986 edition.

The limiter is a one bit A/D converter that outputs 0 when its input is below a threshold value or 1 volt when above the threshold. It is essentially a modification of the threshold logic inverter with a variable threshold parameter.

Figure 5 shows the various switch states as a function of time that were used to design the logic shown in figure 4.

Putting it all together, the PRE_SPICE source code shown in table 1 was used to run the simulation. In this case we ran for a large number of conversion cycles using RELTOL=.01. The large value for RELTOL makes the simulation run faster than the default and we were interested in finding out how simulation accuracy relates to the RELTOL specification.

Table 1, PRE_SPICE Listing for Switched Capacitor A/D Converter	
SWITCHED CAPACITOR A/D	XU4 14 15 9 60 MUX2
.OPTIONS ACCT RELTOL=.01	R60 60 0 1K
+ LIMPTS=513 ITL5=20000	R54 54 0 1K
.TRAN .1US 42US 0 .05US UIC	R55 55 0 1K
*.PRINT TRAN V(7) V(58) V(56) V(9)	R61 61 0 1K
*+ V(10)	XU5 60 53 61 AND2
*.PRINT TRAN V(53) V(3,4) V(6)	*An OR gate when only one
*.PRINT TRAN V(11) V(12) V(13) V(14)	*logic one happens at a time
*+ V(15) V(16)	E13 13 0 POLY(3) 61 0 54 0 55 0 0 1 1 1
.PRINT TRAN V(6) V(3,4) V(53) V(9)	*DUMMY LOADS
*VTST 7 0 PULSE 0 1 1.5US 0 0 4US	R11 11 0 1K
VP1 15 0 PULSE 0 1 .2USEC 0 0 .6US 2US	R12 12 0 1K
VP2 14 0 PULSE 0 1 1.2USEC 0 0 .6US 2US	R13 13 0 1K
VS6 16 0 PULSE 0 1 4.2US 0 0 .6US 4US	R14 14 0 1K
VS2 12 0 PULSE 0 1 .2US 0 0 .6U	R15 15 0 1K
VER 53 0 PULSE 0 1 2US 0 0 2US 4US	R16 16 0 1K
VSM 54 0 PULSE 0 1 5.2US 0 0 .6US 4US	* ANALOG SECTION
VST 55 0 PULSE 0 1 1.2US 0 0 .6US	VREF 1 0 5
VCLR 56 0 PULSE 0 1 .5US	VIN 2 0 1
VONE 57 0 1	XS1 1 3 11 LSWITCH
XU0 0 6 7 LIMITER	XS2 2 3 12 LSWITCH
VFLOP 58 0 PULSE 0 1 1.8US 0 0 1.4US 4US	XS3 0 3 13 LSWITCH
XU1 56 7 58 57 9 10 DFLOP	XS4 4 5 14 LSWITCH
*S1 LOGIC	XS5 4 0 15 LSWITCH
XU2 15 14 9 63 MUX2	XS6 6 3 16 LSWITCH
XU3 63 53 11 AND2	E1 6 0 0 5 1E4
*S3 LOGIC	CF 6 5 10PF
	CI 3 4 10PF
	*INCLUDE THRESH.LIB
	.END



The plot in figure 6, made with Intu_Scope, shows the key circuit waveforms. The error, referred to the input, at the end of the 6th conversion cycle was found to be .11% of full scale. This is strictly a computational error resulting from setting RELTOL=.01.

The OR and AND gates used in this application note used algebraic addition and multiplication respectively in order to reduce the circuit complexity. The switch, LSWITCH, squares up the driving functions to make up for the low gain in the gates.

When substituting MOSFETS for switches and amplifiers it is necessary to use LEVEL=2 and XQC<=.5 to get reasonable results for charge conservation. These model settings will generally produce good results, however, you should run idealized test cases to establish simulation accuracy limits. A future newsletter will discuss charge conservation and related errors.

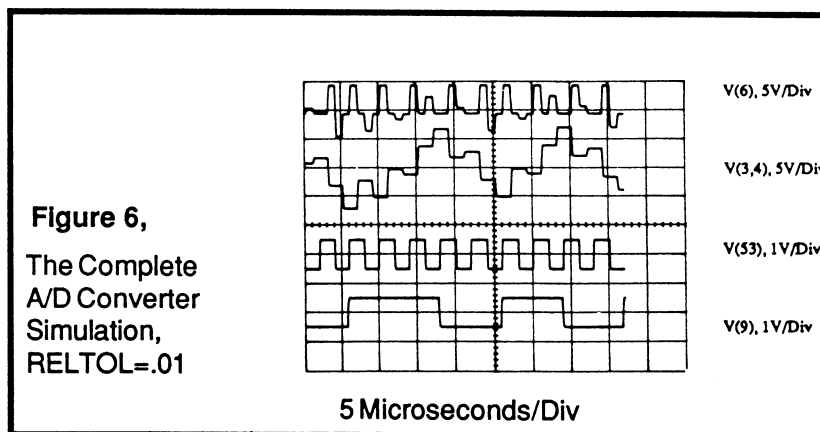


Table 2, Additional Digital Library Models

```
.SUBCKT LSWITCH 1 2 3
*LOGIC INTEFACE 0=OFF, 1E12; 1 = ON,
1K
R1 1 2 1E12
R3 3 0 1E12
E1 4 0 POLY(1) 3 0 0 0 0 0 0 1
R4 4 0 1E6
G1 1 2 POLY(2) 1 2 4 0 0 0 0 1M
.ENDS
*****

.SUBCKT MUX2 1 2 3 4
* SELECT 1 IF 3 TRUE, ELSE 2
X1 1 3 6 AND2
X2 2 8 7 AND2
E1 8 0 0 3 1 1
R3 8 0 1E6
R1 6 0 1E6
R2 7 0 1E6
E2 4 0 POLY(2) 6 0 7 0 0 1 1
.ENDS
*****

.SUBCKT NAND3 1 2 3 4
E1 5 0 POLY(3) 1 0 2 0 3 0 0 1 1 1
G2 0 4 5 0
+ 1.002290E0,2.624314E-3,-1.491959E-1
+ 8.325288E-2,1.321210E0, -3.086306E0,
+ 2.880211E0,-1.322610E0,2.952994E-1,
+ -2.558351E-2,
R1 1 0 1E6
R2 2 0 1E6
R3 3 0 1E6
R4 4 0 1
R5 5 0 1E6
C1 4 0 .87NF IC={IC}
.ENDS
*****

.SUBCKT LIMITER 1 2 3
+ - OUT
* LIMITS OUTPUT TO 0 OR 1 VOLT
RIN1 1 0 1E6
RIN2 2 0 1E6
G1 0 4 1 2 1
D1 4 0 D
D2 0 4 D
.MODEL D D
C1 4 0 1PF
R1 4 0 1E6
E1 3 0 POLY(1) 4 0
+ 5.000000E-1 , 1.974630E0 , 5.437732E-13 , -6.223602E0 ,
+ -2.036383E-12 , 1.202848E1 , 2.807085E-12 , -1.133887E1 ,
+ -1.277173E-12 , 4.059541E0 ,
.ENDS
*****

.SUBCKT AND2 1 2 3
*BE CAREFUL, THIS STAGE HAS UNITY GAIN
RIN1 1 0 1E6
RIN2 2 0 1E6
E1 3 0 POLY(2) 1 0 2 0 0 0 0 0 1
.ENDS
*****

* PIN OUTS FOR 7474
.SUBCKT DFL0P 1 2 3 4 5 6
X1 4 12 11 13 NAND3 {IC=0}
X2 13 1 3 11 NAND3 {IC=1}
X3 11 3 12 10 NAND3 {IC=0}
X4 10 1 2 12 NAND3 {IC=1}
X5 4 11 6 5 NAND3 {IC=0}
X6 5 1 10 6 NAND3 {IC=1}
.ENDS
*****
```

******* SPICE BIBLIOGRAPHY *******

The SPICE Bibliography contains application note references and a continuing list of CAE related publications.

Application note references

- [1] RATIO INDEPENDENT CYCLIC A/D D/A CONVERSION USING RECIRCULATING REFERENCE APPROACH
Shih,C.;Gray,P.;Li,P.
IEEE Transactions on Circuits and Systems
Vol. CAS-30, pp 772-774 October 1983
- [2] SELF CALIBRATION TECHNIQUE FOR A/D CONVERTERS
Lee, H.; Hodges,D.A.
IEEE Transactions on Circuits and Systems
Vol. CAS-30, pp 188-190 March 1983

Reliability and Sensitivity
(These 2 are in our library without a publication reference)

[1] COMPUTER AIDED DESIGN FOR MAXIMUM PRODUCTION
YIELD OR MAXIMUM RELIABILITY

Becker, P.W.; Jensen, F.
Electronics Laboratory
Technical University of Denmark
DK-2800 Lyngby, Denmark

[2] RELIABILITY RELATED TO COMPUTER AIDED CIRCUIT ANALYSIS - A USERS VIEW

Walter, N.A.; Kaposi, A.A.
MIEE C Eng FSS
Kingston Polytechnic
Kingston, Surrey, England

***** **CROSSTALK** *****

Your questions and problems are discussed in a question and answer format.

Q. Explain your Monte Carlo Package, does it allow user definable distribution? How many simulations can be run? What is the output? Can tolerances be given to each component?

A. The following summarizes the Monte Carlo Analysis features:

- The default distribution function is Gaussian, It can be replaced with a user definable function.
- Simulations are run for a number of Lots and a number of Cases within a lot with statistics defined by DEV=value for case runs and LOT=value for different lots. You can run up to 999 lots and 999 cases within each lot which generally exceeds both run time and memory limitations of the PC.
- Outputs are saved in a subdirectory file called MONTE.OUT. This file is created using Intu_Scope, the graphics post processor in a programmed mode. Any measurement that can be placed in the Intu_Scope accumulator can be saved. We have measured gain margin, phase margin, pass band ripple, propagation delay and rise time. You could also make weighted measurements such as the sum of squares of rise times, or use our FFT to measure spectral

energy over some bandwidth. The circuit performance functions which can be recorded and analyzed are essentially unlimited.

- Outputs are displayed and measured using Intu_Scope. Two special grids are available. The probability grid plots the cumulative probability of the output data on a nonlinear grid, producing straight line plots for gaussian distributions. The histogram grid is a bar chart that automatically selects 0.5 sigma cell widths. Both grids provide mean and standard deviation displays.
- Tolerances can be applied singly to any parameter or generically to a component type by naming the type following the parameter, for example [RN60] for a resistor [PSTOL] for your power supplies, or TOL=1MV to a voltage source. When values are specified using the postfix %, the tolerance is taken as a percent of the value. When the % is not used, the tolerance is an absolute value.
- When devices are specified using “.SUBCKT” or “.MODEL” calls, then you can use the parameter passing features of the program to automatically create a new device each time the parameter list is different.

Q. Sometimes I get a “real indefinite” error message with no output file. Is there any way to get the output data?

A. If the error occurs during the transient analysis, then you can note the simulation time at which the error occurred and run again, this time press ESC just before the fatal error and the output will be printed up to that time. The “real indefinite” error occurs when operations such as 0.0/0.0 are attempted. This may happen when initial conditions are not completely specified with a UIC directive in the “.TRAN” statement. One rather simple circuit in which this occurs is shown below. If no IC is given for L1 or if IC=0 is used the analysis will not run. Any non zero initial condition gets out of the problem.

```
TEST CIRCUIT
.PRINT TRAN V(1) V(2)
.TRAN 5US 500US UIC
CIN 1 0 1U IC=10
L1 1 0 1MHY IC=1E-15
L2 2 1 4MHY
K12 L1 L2 .95
RL 2 0 1K
.END
```