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*Personal Computer Circuit Design Tools*

# N E W S L E T T E R



*** * * * * APPLICATION NOTE * * * * ***

## SWITCHED CAPACITOR NETWORK MODELS

This issue and the next newsletter will feature a two part discussion of modeling Switched Capacitor Networks (SCN's).

The motivation for developing these models is to show how a general class of sampled data problems can be formulated using Z transform theory and simulated using IS_SPICE.

When switched networks are modeled using standard IS_SPICE elements for switches, the resulting circuit can only be run in time domain to produce a transient analysis. The AC analysis features will not work because the switches will be linearized in one position or the other, resulting in no signal transmission. Frequency response can be found by using the fourier transform of a pulse driven simulation. The pulse simulation must run for many pulse width's and a large number of computations are required over each pulse interval. The transient simulation can take hundreds of times longer than an equivalent AC analysis.

If the switching operation can be represented using continuous time elements, then the AC analysis features of IS_SPICE can be used to save computational time. The saving in computational time makes extraction of Monte Carlo sensitivities practical.

It is well known that sample data systems can be converted to "frequency" domain using the Z transform to represent the sampling and switching. The Laplace operator, $e^{st}$, is defined to be Z, the equivalent Z transform operator. The presence of a transmission line model in IS_SPICE makes a continuous time representation possible for IS_SPICE simulation, since a terminated transmission line is the time domain equivalent of $Z^{-1}$.

To get to a continuous model, it is first necessary to construct an equivalent circuit representation using sampled data theory. The work presented by Laker [1] develops these models for two phase switched networks. The underlying assumptions are:

1. The time varying SCN consists of 2 networks, one for each clock phase, coupled topologically into one network representation.

2. Network equations are formulated based on charge conservation, therefor, current in the IS_SPICE simulation is the analog of charge.

The second assumption limits the simulation outputs and interaction with other continuous time elements to node voltages that correspond to low impedance sources. Remember that current in the equivalent circuit is used to represent charge. It is not permissible to use a continuous time op-amp connected to the charge port of a simulated switch!

The networks in figures 1 and 2 show the formulation for a floating capacitor and a toggle switched capacitor. Notice that there are several new circuit elements, the "Storistor" and a resistor whose value is inversely proportional to capacitance.

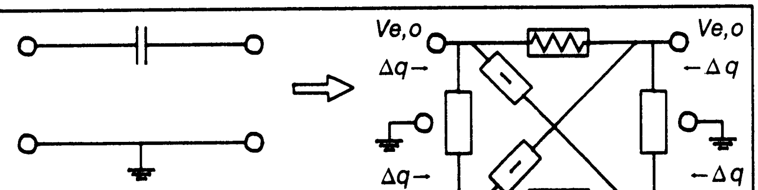



**Figure 1, Floating Capacitor Equivalent Circuit**

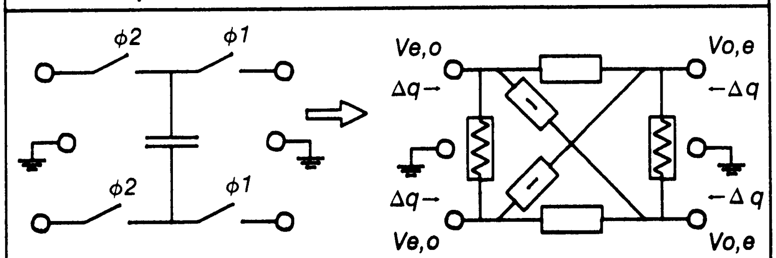


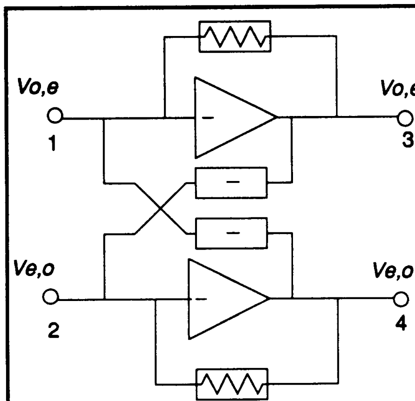

**Figure 2, Toggle Switch Equivalent Circuit**

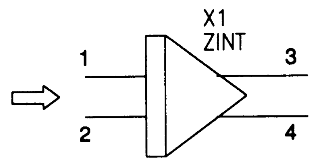
The storistor is a resistor that transfers charge (current in the IS_SPICE analog) after a time delay. The Storistor is bidirectional and can be positive or negative.

These new elements are scaled so that the current falls in a reasonable range. If current and charge were scaled equivalently, the current that represents charge in the models would be extremely small and require changes to some of the default IS_SPICE options.

The SCN integrator shown in figure 3 combines the floating capacitor with a charge amplifier. The charge amplifier is the equivalent of a SCN op-amp. Notice that the elements connected between outputs and between virtual grounds were eliminated since they do not contribute to the voltage transfer function.

Figure 4 shows how a parasitic insensitive switch is connected to make an integrator that sums inputs taken from the odd port and subtracts inputs at the even port. Elements connect between ground and virtual ground or between voltage sources are removed. Only two elements remain in the toggle switch model after this simplification.




```
.SUBCKT ZINT 1 2 3 4
* 2 PHASE INT,
*1 3 ODD IN->OUT; 2,4 EVEN
R1 1 3 {1E-9/C}
R2 2 4 {1E-9/C}
E13 3 0 1 0 -1E6
E24 4 0 2 0 -1E6
G14 1 4 0 31 {C*1E9}
R14 31 0 1000
T14 30 0 31 0 Z0=1000 TD={TD}
E14 30 0 1 4 1
G23 2 3 0 41 {C*1E9}
R23 41 0 1000
T23 40 0 41 0 Z0=1000 TD={TD}
E23 40 0 2 3 1
.ENDS
```

**Figure 3, IS_SPICE Integrator Model**

A library of useful parts is shown in figure 5. These parts can be used to build a continuous time equivalent circuit for most common SCN 2 phase circuits. The PRE_SPICE parameter passing capability is used to generalize the parts and scale the transmission line termination to be in the range of impedance used elsewhere in the circuit.

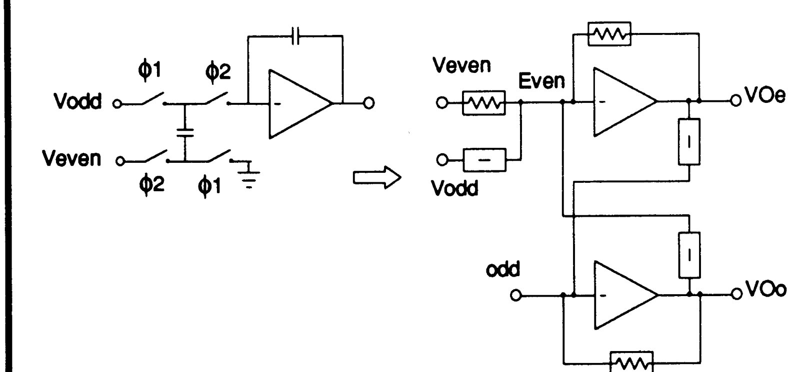



**Figure 4, Parasitic Insensitive SCN Integrator**

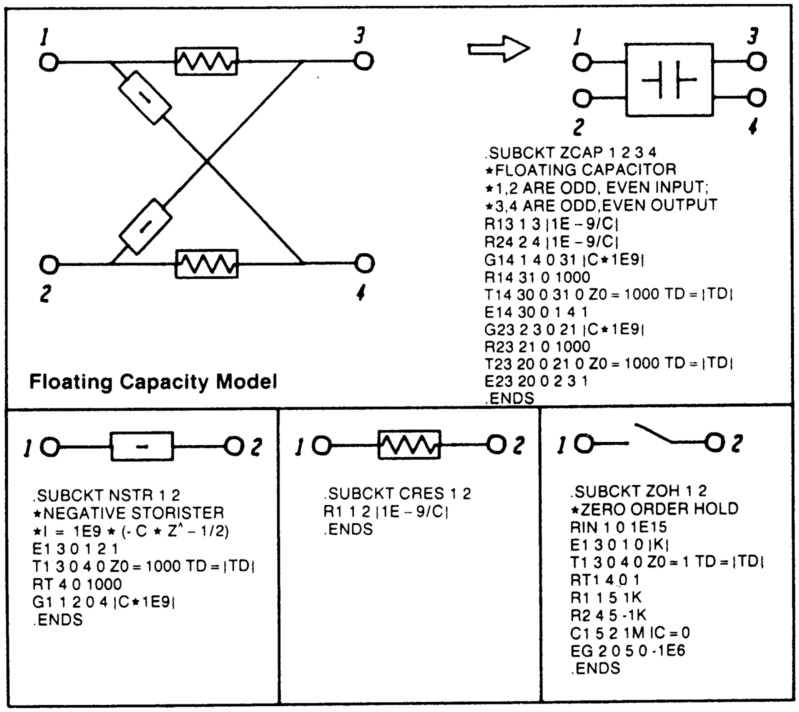



**Figure 5, Basic Z-Transform Elements Models**

When constructing an equivalent circuit, it is convenient to use even node labels to identify even switched ports and odd numbers for odd switched ports. A standard inverting integrator is then formulated by connecting a CRES element from an even port to the even integrator input. A positive summation occurs when a PSTR element is connected from an even output port to the odd input port. Floating capacitors are 4 ports devices, ZCAP, that connect from even,odd outputs to even,odd inputs. We will assume that even ports switch first, so that an odd port that is not available can be made by processing the voltage through a time delay, UTD. If the system output is run through a sample and hold, then a zero order hold, ZOH, should be added to the output.

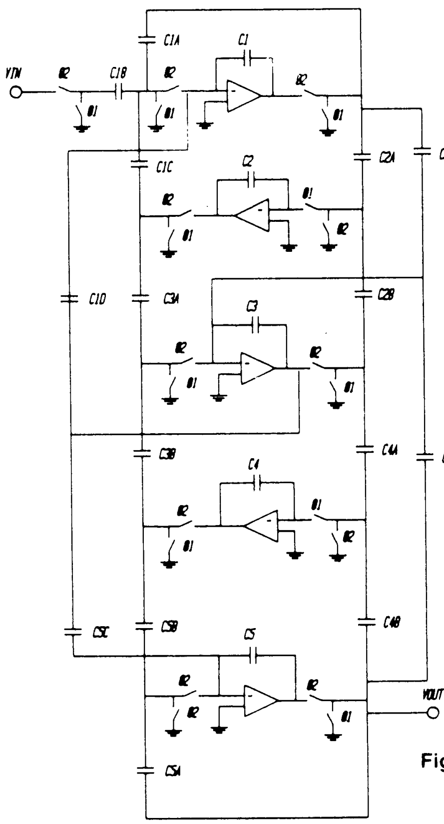
Figure 6 shows a fifth order elliptic filter described in Gregorian and Temes [2] and its continuous time equivalent. The PRE_SPICE listing shown next generated the output which was plotted using Intu_Scope in figure 7.

## PRE_SPICE SOURCE FOR ELLIPTIC FILTER SCN

```
5TH SCN ORDER ELLIPTIC FILTER

.AC DEC 50 .1K 1MEG
.PRINT AC VM(4) VP(4) VM(8) VP(8) VM(12) VP(12)
.PRINT AC VM(16) VP(16) VM(20) VP(20)

VIN 1 0 PULSE 0 1 AC 1

X1 2 3 4 5 ZINT {C=13.87171PF [SCAP] TD=1US}
X2 6 7 8 9 ZINT {C=11.11901PF [SCAP] TD=1US}
X3 10 11 12 13 ZINT {C=14.46156PF [SCAP] TD=1US}
X4 14 15 16 17 ZINT {C=14.43078PF [SCAP] TD=1US}
X5 18 19 20 21 ZINT {C=8.27441PF [SCAP] TD=1US}
XC2A 4 7 NSTR {C=1.20275PF [SCAP] TD=1US}
XC2B 7 12 NSTR {C=1PF [SCAP] TD=1US}
XC4A 12 15 NSTR {C=1.52861PF [SCAP] TD=1US}
XC4B 15 20 NSTR {C=1PF [SCAP] TD=1US}
XC1A 4 2 CRES {C=1.83854PF [SCAP] TD=1US}
XC1B 1 2 CRES {C=1PF [SCAP] TD=1US}
XC1C 2 8 CRES {C=1.77112PF [SCAP] TD=1US}
XC3A 8 10 CRES {C=1PF [SCAP] TD=1US}
XC3B 10 16 CRES {C=1.14172PF [SCAP] TD=1US}
XC5B 16 18 CRES {C=2.02212PF [SCAP] TD=1US}
XC5A 18 20 CRES {C=1PF [SCAP] TD=1US}
XC1D 3 2 13 12 ZCAP {C=1.90667PF [SCAP] TD=1US}
XC3C 5 4 11 10 ZCAP {C=1.29480PF [SCAP] TD=1US}
XC5C 19 18 13 12 ZCAP {C=5.67396PF [SCAP] TD=1US}
XC3D 21 20 11 10 ZCAP {C=2.09575PF [SCAP] TD=1US}

*TOL SCAP LOT=30% DEV=2%

*INCLUDE SCN.LIB
.END
```

Next, a Monte Carlo analysis was run to check pass band ripple and stop band attenuation. The capacitor tolerance matching was taken to be 2% and circuit to circuit variations were taken as 30%. An 82% yield was computed for a pass band ripple tolerance of 0.1 dB and the yield for 39 dB stop band attenuation was 90% based on a sample of 60 circuits.

The next news letter will continue the development of SCN modeling to time domain macro models, showing a switched capacitor A/D converter with mixed analog and digital components.



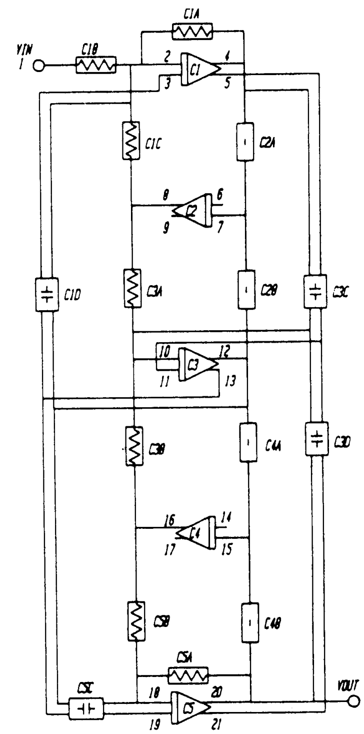


**Figure 6, A Fifth Order SCN Elliptic Filter Schematic and its continuous time equivalent circuit**

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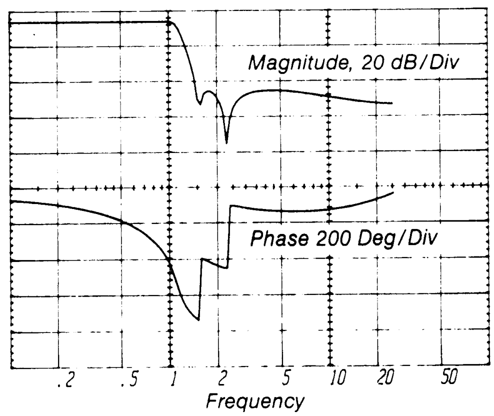


**Figure 7, Frequency Response of the Continuous Time Equivalent Circuit**


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## * * * * * CROSSTALK * * * * *

A question and answer format is used to describe typical problems and their solutions.

Q. Why doesn't IS_SPICE take the time steps I specify?

A. The time steps are automatically selected based mainly on a local truncation error (LTE) of integration. Local truncation error is the difference between the exact solution and the numerical solution at the next time step. When the error is estimated to be excessive, the program will automatically reduce the time step and conversely increase the step for small errors. The RELTOL specification in the ".OPTIONS" statement controls this parameter. You can force a maximum time step using the ".TRAN" statement optional parameters. The minimum is a function of LTE or an absolute minimum that signify's convergence failure.

Q. Why are simulation results more accurate than the RELTOL specification?

A. As mentioned above, RELTOL is used to control the integration step interval. The fastest changing state variable will control the entire solution. Moreover, the final value of the integration may be more accurate than the intermediate steps.

Q. What is the source of error in the printout of transient driving functions?

A. This occurs when the time step is too large. The print time step is specified in the ".TRAN" statement, however, as described above the time step is based on integration errors. If you run an analysis that involves little or no integration error, then the analysis time step could be large compared to the change in a driving function. IS_SPICE computes the output using linear interpolation between analysis points. To solve the problem you must reduce the maximum time step using the ".TRAN" statement options.

Q. How can I tell if a mainframe SPICE problem can run on the PC?

A. Use the ACCT keyword in the ".OPTIONS" statement to see how much memory you use. IS_SPICE has a MAXMEM of 40000. If the memory use listed under MEMUSE is less, then the simulation will run using IS_SPICE on a PC. The memory words in this context are 32 bits long, therefor, IS_SPICE reserves 160K Bytes for solving the simulation problem.

Q. How can I use a mainframe to run Monte Carlo analysis using PRE_SPICE and Intu_Scope?

A. We recommend running all Monte Carlo cases in batch mode on the mainframe. This can be done be first running MONTE.EXE instead of PRE.EXE. This generates all of the source files. These files can then be transferred to the mainframe and run in batch mode. The output file names will then be of the form LnCm.OUT, where n and m run from 1 to the specified number of lots and cases. These files can then be moved to the analysis directory and the batch file MSPICE.BAT can be replaced with a null file since the analysis is already finished. Then you can run PRE.EXE as you would normally and the IS_SPICE analysis is omitted. This procedure will of course require enough PC memory to hold all of the ".OUT" files. If you have a reasonable network tie, you can alter MSPICE.BAT to call for the mainframe analysis as you go, an alternative that uses less memory since the output files are deleted after the Intu_Scope data reduction.

Q. How can group delay be measured?

A. Group delay is defined as d(Phase)/d(Frequency). You must do this using Intu_Scope with a linear grid. If phase is in Radians and Frequency is Radians/Sec, the result is time, in Sec's. IS_SPICE outputs are in Degrees and Hertz, so that you must divide the output by 360 to convert to time (Sec = degrees/(360_Degrees/Hertz). Intu_Scope 1.2 will assign incorrect units and vers 2.0 will remove the units.