intusoft (310) 833-0710 *Personal Computer Circuit Design Tools*

N E W S L E T T E R

******* APPLICATION NOTE, AN ELLIPTIC FILTER *******

This application note gives an example of the capabilities of the Intusoft circuit design tools, showing some of the analyses that compliment a breadboard evaluation and others that would not have been done without the availability of computer simulation. The circuit chosen to illustrate these capabilities is a fifth order elliptic filter. Shown in figure 1, the filter is used for a sampled data system anti-aliasing filter. The purpose of an anti-aliasing filter is to limit the bandwidth of incoming information so that the sampling process will not fold high frequency data back into the pass band, potentially giving erroneous results. The PRE_SPICE source listing is shown in table 1 at the end of the application note.

The topology uses an inverting amplifier in the first stage to provide gain and the first stage roll off. The remaining stages use unity gain amplifiers to provide pairs of complex poles and zeros. Low Q sections are cascaded first in order to minimize interstage overshoot, thereby maximizing dynamic range. Simulation results will be used to predict the effect of amplifier noise,

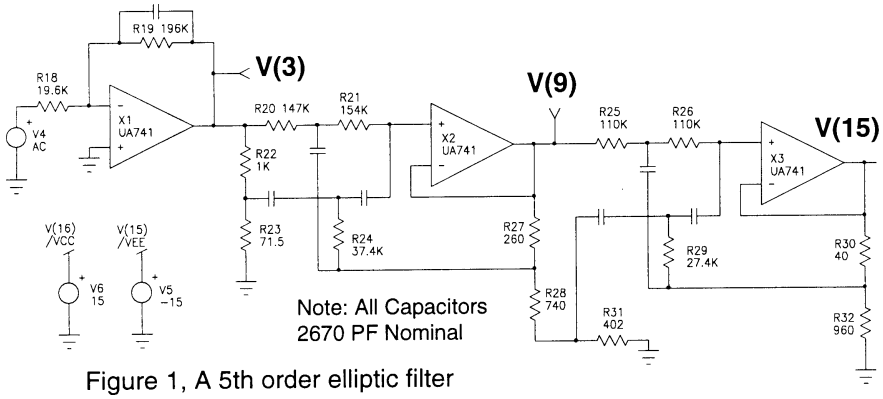

Figure 1, A 5th order elliptic filter

determine the filter overshoot from a step input and find the time to recover from an input overdrive. Monte Carlo analysis will be used to refine component values and define performance parameters.

The filter was synthesized to have pass band ripple of .5dB with the transition ratio, R, [Fcutoff / F(-.5dB)] set to 1.75 and the stop band attenuation set to 60dB. The parameters were padded slightly because production tolerances and temperature variations are expected to deterio-

rate performance. The over shoot will set dynamic range limits and will be determined by breadboard or simulation measurement in order to avoid spending excessive time solving the differential equations.

The circuit cost and performance is driven by the accuracy of the capacitors. In order to reduce cost, it was decided to group capacitors in matched sets. The matching criteria was set to 1% with an additional 1% tolerance for soldering, aging and thermal effects. This technique maintains the ripple, attenuation and transition ratio with tight tolerances while letting the pass band frequency have the wider tolerance.

This filter is used in conjunction with a digital filter that eliminates data above some frequency, F1. The sampling frequency is 2 * Fn, where Fn is the nyquist frequency and is given by:

$$Fn = 0.5 * (Fc + F1) = 0.5 * (Fp * R + F1)$$

The cutoff frequency, Fc, folds back to F1 and requires that frequencies between F1 and Fn be discarded by the digital filter. Once Fn is selected, component variations cannot cause Fp, the passband frequency, to be less than F1 (excessive pass band ripple), moreover, F1 cannot exceed 2 * Fn-Fc or out of band information will alias into the passband. The sampling frequency is established by solving

$$2 * Fn = Fcmax + Fpmin$$

using Monte Carlo analysis data. This will also set F1, the useful bandwidth. The capacitor values can then be rescaled to force either F1 or the sampling frequency toward a specified value. The tolerances to be found by the Monte Carlo analysis are then:

Pass band frequency, Fp	Stop band frequency, Fc
Stop band attenuation	Transition Ratio
Pass band ripple	

The last 2 parameters are input parameters for the filter design and will be needed if the filter proves unacceptable and another cut is required. Before the Monte Carlo analysis is performed, the transient and noise analysis will be used to test for any unexpected results. These analyses are performed using the nonlinear device representation for the operational amplifier. The transient response shows maximum overshoot at the output stage of 15% and a well behaved recovery from a saturating input in figures 2 and 3.

Noise performance is shown in figure 4. The sharp cutoff in output noise in the stop band is necessary to limit the broad band noise aliasing into the pass band by the sample and hold. Noise peaking is occurring for frequencies rejected by the digital filter. Key values were measured using Intu_Scope and are summarized in the figures.

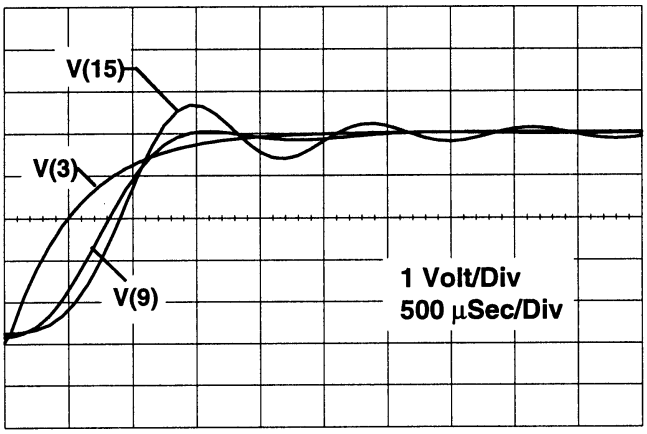

Figure 2, Filter response to a step input

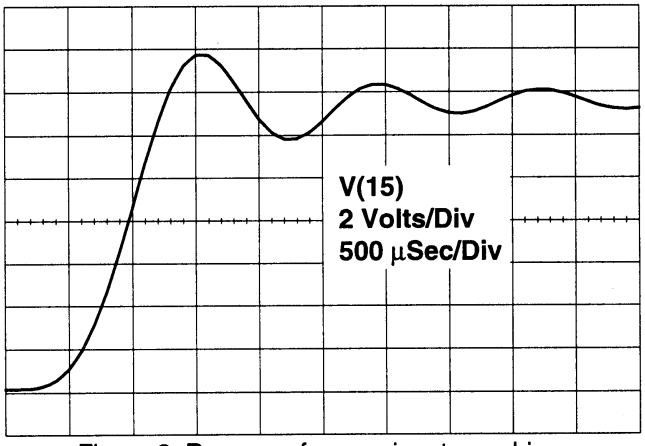

Figure 3, Recovery from an input overdrive

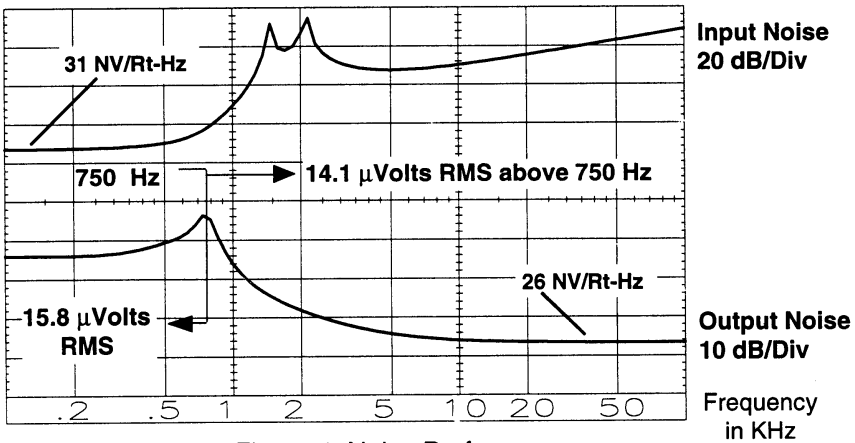

Figure 4, Noise Performance

To give some idea of the analysis capabilty on a PC, the AC analysis in this example required 115 seconds to run on a standard PC-AT, had 33 nodes, and used 18% of the memory reserved for matrix operations. The Monte Carlo analysis took 75 minutes for 30 runs.

Monte Carlo analysis was performed using the linear circuit models for the amplifiers in order to minimize run time. The results are summarized below based on 30 trial runs. A nominal case is shown in figure 5.

Monte Carlo Simulation summary (30 Cases)

		(.. 3 Sigma limits ..)		
Parameter	**nominal**	**min**	**max**	**tolerance**
Passband frequency	**759Hz**	**667Hz**	**851Hz**	**12%**
Stopband frequency	**1370Hz**	**1212Hz**	**1527Hz**	**11.5%**
Stopband attenuation	**60.1dB**	**59.5dB**	**60.8dB**	**.67dB**
Transition ratio	**1.8**	**1.726**	**1.874**	**4.1%**
Passband ripple			**1.5dB**	

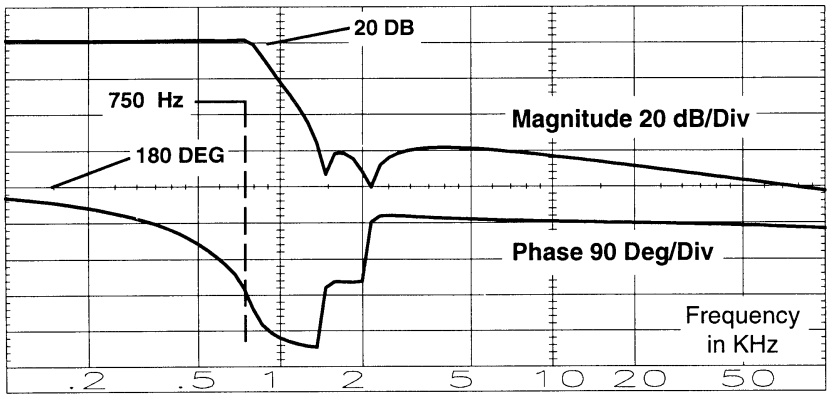

Figure 5, Nominal case frequency response

CONCLUSION: The computer simulation has been shown to be an effective way to establish design parameters and perform trade offs that can be used in the pre-breadboard phase of a design to establish both design requirements and address economic issues. The breadboard or prototype when used in this context becomes a tool to validate the analytical assumptions. This approach to circuit design reverses the traditional role of breadboard and analysis, eliminating neither; but rather, using the best features of both.

Table 1, PRE_SPICE source for an elliptic filter

```
5th order elliptic filter
*.AC DEC 30 100 100K
.TRAN 50US 5MS
.PRINT AC V(15) VP(15) V(9) V(3)
.PRINT TRAN V(15) V(9) V(3)
VIN 1 0 AC 1 PULSE 5 0 0 0 0 5MS
VCC 77 0 15
VEE 44 0 -15
R1 1 2 19.6K [RN60]
R2 2 3 196K [RN60]
X1 2 0 3 77 44 UA741
R3 3 5 147K [RN60]
R4 5 8 154K [RN60]
R6 3 4 1K [RN60]
R7 4 0 71.5 [RN60]
R8 6 7 37.4K [RN60]
X2 9 8 9 77 44 UA741
R9 9 7 260 [RN60]
R10 7 10 740 [RN60]
R11 10 0 402 [RN60]
R12 9 11 110K [RN60]
R13 11 14 110K [RN60]
R14 12 13 27.4K [RN60]
R15 13 0 960 [RN60]
R16 13 15 40 [RN60]
X3 15 14 15 77 44 UA741
XNET 2 3 4 5 6 7 8 10 11 12 13 14 CNET {FREQ=750}
*CAPACITORS PLACED IN SUBCKT SO THEY CAN BE SCALED
*FOR DIFFERENT BANDWIDTH, SET BY THE PARAMETER FREQ
.SUBCKT CNET 2 3 4 5 6 7 8 10 11 12 13 14
C1 2 3 {2U/FREQ} [CKO7]
C2 4 6 {2U/FREQ} [CKO7]
C3 6 8 {2U/FREQ} [CKO7]
C4 5 7 {2U/FREQ} [CKO7]
C5 10 12 {2U/FREQ} [CKO7]
C6 12 4 {2U/FREQ} [CKO7]
C7 11 13 {2U/FREQ} [CKO7]
.ENDS
*TOL RN60 LOT=0% DEV=1%
*TOL CKO7 LOT=10% DEV=2%
*INCLUDE NONLIN.LIB
.END
```

********* CROSS TALK *******

A discussion of models and techniques for using SPICE prompted by questions from Intusoft customers are provided in this section.

Q. How can a switch be modeled ?

A. Use a voltage source in the PULSE mode to control an active element. One simple but effective element is a voltage controlled current source,

connect back to itself to make a resistor. The resistor value can be varied to turn the switch on or off using the POLY keyword as illustrated below.

```
* OPEN WHEN V(3,0) = 0, CLOSED WHEN V(3,0) <> 0
* ON RESISTANCE IS 1/V(3)
* OFF RESISTANCE 1E12
.SUBCKT SWITCH 1 2 3
R1 1 2 1E12
G1 1 2 POLY(2) 1 2 3 0 0 0 0 0 1
.ENDS
```

Q. Where do I find error messages ?

A. Error messages are found in the IS_SPICE "*.OUT" file unless the program was stopped by a compiler run time error. Run time errors are rare and usually confined to problems that can be classified as convergence related errors. The "*.OUT" file will not be present when a compiler run time error is encountered, so you must resort to rechecking topology or reducing the circuit into several smaller circuits for debugging.

Q. Why don't coupled inductors run ?

A. They do! Coupled inductors bypass the SPICE error check that rejects loops of inductors. The reason for this rule is that the initial current is indeterminite (0 ohms / 0 Volts). Using some series resistance or starting the analysis with power off solves the problem. Make sure your initial conditions result in defining a unique operating point; for example, a C-L-C pi section with initial capacitor voltages that are equal will also require specification of inductor current or series resistance. If your initial conditions are in conflict, there may be a convergence problem.

Q. What should I do when the program stops with a convergence error message?

A. Convergence errors are caused by either numerical instability or by a multi-valued circuit such as an oscillator or flip-flop.

The NODESET directive will help SPICE find the "correct" initial condition by starting the search for a steady state solution in the neighborhood of the operating point you desire.

Astable circuits will not converge so that you must use the UIC keyword in the ".TRAN" statement and provide initial conditions for capacitor voltage and inductor current. The transient initial conditions will then be forced to these values.

Numerical instability occurs either dynamically or in computing the DC steady state operating point. Strong nonlinearities such as diodes are primarily responsible for this problem. These nonlinearities can be “softened” by adding resistance, say 1E10 ohms, across the diode or in the transient analysis by adding a reasonable capacitance across the diode. The capacitance is frequently more effective and the DC solution can be circumvented by starting the simulation with power off, thereby making the initial currents all zero. A power on step is then used to start the analysis.

Q. What is the difference between NODESET and initial conditions?

A. When you define initial conditions without the UIC keyword, they are taken to be the same as NODESETS and are used to begin a search for the steady state solution. The transient analysis will not necessarily begin with the NODESET or initial condition values. When UIC is specified, the initial conditions are used to begin the analysis. NODESET's cannot be used within a subcircuit; however, initial conditions can be specified and passed as parameters using PRE_SPICE.

Q. What do I do when the analysis stops because the time step is too small?

A. SPICE varies the time step dynamically based on local truncation error limits that can be set in the “.OPTIONS” statement. The RELTOL parameter can be increased, usually up to .01 without problems, in order to get by “time step too small” errors. These errors are frequently caused by excessive circuit simplification; for example, a sudden change in inductor current without having any capacitance or resistance will result in ringing at infinity. There is no time step small enough to satisfy the nyquist stability criteria for ringing at infinity and the analysis will abort. Providing damping for inductors and capacitors and reasonable capacitance across diodes will eliminate most of these problems.

Q. Why do I see ringing or limit cycles in the analysis that don’t seem right?

A. Numerical solution of the differential equations that describe your circuit results in a sampled data control system. There is no way to predict stability because of the non linearities of the circuit and the variable time step. You may find numerical artifacts in your data; for example, ringing or a limit cycle that is not reasonable. The time step can be forced to a smaller value in the “.TRAN” statement or stability constraints can be changed by switching to the GEAR integration routine using the “.OPTIONS” statement. As circuit complexity increases, the time step will usually shorten enough to satisfy stability considerations, making the increased speed of the default trapezoidal integration a better choice.