intusoft

Personal Computer Circuit Design Tools

N E W S L E T T E R

The OP-AMP model provided in most SPICE packages was found to have serious flaws:

1. No output inductance
2. No summing junction capacitance
3. Load current not reflected to power lines

These oversights would incorrectly predict stable circuit operation for certain capacitive loads or high impedance feedback networks. Some power buffer topologies could not be simulated because they use load reflected power line current. To resolve these problems, **intusoft** developed a *new* generic OP-AMP model for PRE-SPICE and included information on selecting parameters. It is used for the UA741 model in the libraries and is the subject of this issues application note.

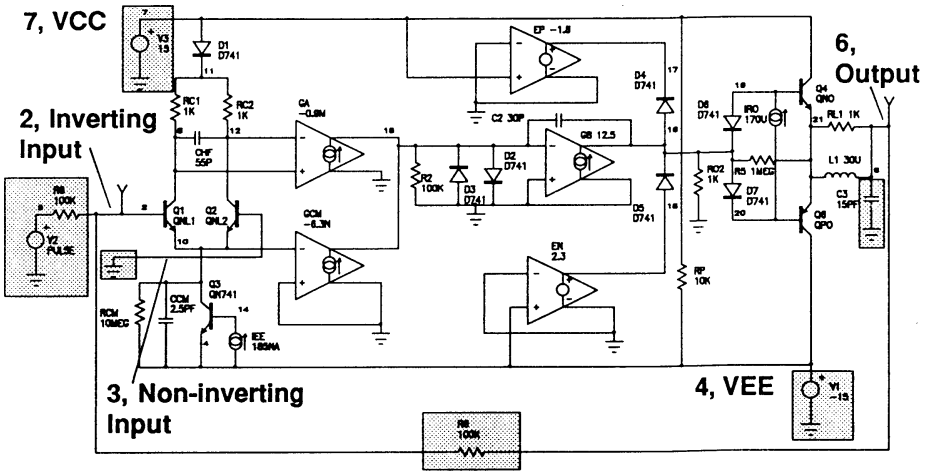
APPLICATION NOTE: OP-AMP MODELS

GENERIC BIPOLAR OP-AMPS: Parameters common to many OP-AMPS can be modeled using similar techniques. A generic model has been created for OP-AMPS that are constructed using bipolar technology. Besides modeling the linear and DC transfer function, the non linear model includes the following parameters.

- Input stage non linearities
- Input voltage and current offsets and bias
- Slew rate limiting
- Common mode gain
- Power supply rejection
- Output current limiting
- Output voltage limiting
- Reflection of load current to power input
- Output stage non linearities

The equivalent circuit shown in figure 1 takes advantage of the idealized device behavior possible through simulation. Parameters are defined for the three stages of the simulated amplifier.

Input Stage: The input non linearities are simulated using Q1, Q2, Q3 and D1. These are set up to simulate the topology for a 741 or similar amplifier with respect to bias and common mode range. The input transistors, Q1 and Q2, should be modeled to reflect the performance characteristics of the op amp so that bias current, offset current and offset voltage are modeled. Noise parameters can also be modeled in this stage. RCM and CCM will convert common mode signals to differential signals and also couple power line variations into the input. The high frequency pole is modeled with RC1, RC2 and CHF. Values of RC1 and RC2 must be small in order to get the input capacitance of Q1 and Q2 to provide reasonable high frequency behavior. Q1 and Q2 are made slightly different to develop input offsets, and their emission coefficients can be selected to simulate the effect of other transistor cascades in the input and slew rate limiting.




```
.SUBCKT UA741  2   3   6    7    4
*                    - IN + OUT VCC VEE
.MODEL QN741 NPN
.MODEL D741 D(CJO=3P)
D1 7 11 D741
RC2 11 12 1K
RC1 11 8 1K
CHF 8 12 55P
Q1 8 2 10 QNL1
.MODEL QNL1 NPN(NF=1.5
+  BF=111 IS=8E-16 CJE=3P)
Q2 12 0 10 QNL2
.MODEL QNL2 NPN(NF=1.5
+ BF=144 IS=8.3E-16 CJE=3P)
Q3 10 14 4 QN741
CCM 10 4 2.5PF
IEE 4 14 185NA
GA 0 15 8 12 -0.9M
GCM 0 15 0 10 -6.3N
R2 15 0 100K
D2 15 0 D741 OFF
D3 0 15 D741 OFF
GB 0 16 0 15 12.5
D4 16 17 D741 OFF
D5 18 16 D741 OFF
EP 17 0 7 0 -1.8 1
EN 18 0 4 0 2.3 1
D6 19 16 D741 OFF
D7 16 20 D741 OFF
Q4 7 19 21 QNO
.MODEL QNO NPN(BF=150 IS=1E-14)
Q6 4 20 21 QPO
.MODEL QPO PNP(BF=150 IS=1E-14)
L1 21 6 30U
C3 6 0 15PF
RL1 21 6 1K
R5 16 21 1MEG
IRO 20 19 170U
V1 4 0 -15
R6 2 6 100K
RCM 10 4 10MEG
R8 5 2 100K
V2 5 0 PULSE 0 5 0 0 0 25U
C2 15 16 30P
RP 7 4 10K
RO2 16 0 1K
V3 7 0 15
.END S
```

Figure 1, A generic Op-amp Equivalent Circuit; shaded areas contain components external to the actual op-amp model and are used for simulation purposes only.

Slew rate limiting is set by this stage. The large signal output voltage is limited to BETA3*IEE*RC and the small signal gain is RC*.5*BETA3*IEE/(NF*VT). If the small signal output is integrated to provide a unity gain cross over at the radian frequency Wt, the the slew rate is:

dV/dT = 2*NF*VT*WT

The emission coefficient, NF, then sets the slew rate limit or you could add emitter resistance as done in some other models, however, modifying N uses fewer nodes. To make the slew limit unsymmetrical you can unbalance the collector resistance RC1 and RC2.

Interstage: Controlled sources GA and GCM couple the differential and common mode signals to the interstage amplifier, GB. The DC gain is given by:

Adiff = RC*.5*(BETA3*IEE/(NF*VT))*GA*R2*GB*RO2

At frequencies below the pole at W = 1/(2*RC*CHF), the gain is given by:

Adiff(mid freq) = RC*.5*(BETA3*IEE/(NF*VT))*GA/(jW*C2)

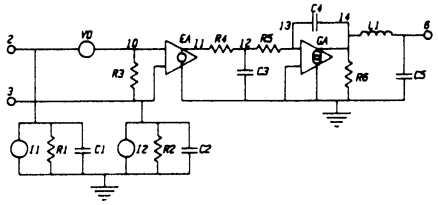
and the unity gain frequency is approximated by solving for W when Adiff = 1.

Two non linearities are modeled in the interstage. First, the large signal overshoot is limited by diodes D2 and D3. For amplifiers where this is caused by a pair of diodes, then the emission coefficients of the diodes can be adjusted. The second non linearity is the output swing which is taken as a constant value subtracted from the power rails. D4, D5, EP and EN act as output limiters. It is important to return the limited current to the subcircuit ground node so that the source, GB, does not generate any apparent power.

Static power dissipation is modeled using resistor RP connected across the power lines.

Output Stage: The output stage is modeled using D6, D7, Q4, Q5 and L. The transistors are not given any AC parameters, instead a discrete inductor simulates the AC performance while the transistor BETA and the source IRO account for both current limit and output resistance. This stage will return the load current to the power lines, enabling simulation of certain power stage configurations.

741 OP-AMP: The 741 OP-AMP is a high performance monolithic Operational Amplifier used in many of todays electronic products. Figure 1 gives the full nonlinear model schematic and listing. A simplified model that excludes nonlinear elements is given in figure 2. Figure 3 shows how the models predict instability when the amplifier is improperly loaded.



```
.SUBCKT UA741 2    3    6    7    4
              -IN  +IN  OUT  VCC  VEE
RP 4 7 10K
RXX 4 0 10MEG
*
IBP 3 0 80NA
RIP 3 0 10MEG
CIP 3 0 1.4PF
IBN 2 0 100NA
RIN 2 0 10MEG
CIN 2 0 1.4PF
VOFST 2 10 1MV
RID 10 3 200K
EA 11 0 10 3 1
R1 11 12 5K
R2 12 13 50K
C1 12 0 13PF
GA 0 14 0 13 2700
C2 13 14 2.7PF
RO 14 0 75
L 14 6 35UHY
CL 6 0 3PF
.ENDS
```

Figure 2, A linear UA741 model

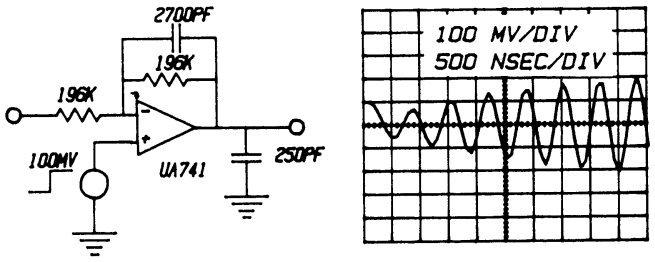


Figure 3, OP-AMP Model Predicts Instability