Average simulations of FLYBACK converters with SPICE3

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Within the wide family of Switch Mode Power Supplies (SMPS), the Flyback converter represents the preferred structure for use in small and medium power applications such as wall adapters, off-line battery chargers, fax machines, etc. The calculations involved in the design of a Flyback converter, especially one which operates in discontinuous mode, are not overly complex. However, the analysis of the impact of the environment upon the system may require a lengthy period of time: ESR variations due to temperature cycles, capacitor aging, load conditions, load and line transients, the effects of the filter stage, etc. must be considered.

A SPICE simulator can help the designer to quickly implement his designs and show how they react to real world constraints. The simulation market constantly releases SMPS models, and the designer can rapidly lose himself in the eclecticism of the offer. This article will show how you can benefit from these new investigation tools.

Simulating SMPS with SPICE is not a new topic

In 1976, R. D. Middlebrook settled the mathematical basis for modeling switching regulators [1]. Middlebrook showed how any boost, buck, or buck-boost converter may be described by a canonical model whose element values can be easily derived. In 1978, R. Keller was the first to apply the Middlebrook theory to a SPICE simulator [2]. At that time, the models developed by R. Keller required manual parameter computation in order to provide the simulator with key information such as the DC operating point. Also, the simulation was only valid for small signal variations and continuous conduction mode.

Two years later, Dr. Vincent Bello published a series of papers in which he introduced his SPICE models [3]. These models had the capacity to automatically calculate DC operating points, and allowed the simulated circuit to operate in both conduction modes, regardless of the analysis type (AC, DC or TRAN). Although these models are 15 years old, other models have been introduced since then, our example circuits which have been based upon them will demonstrate how well they still behave.

Switching or average models ?

Switching models will exhibit the behavior of an electrical circuit exactly as if it were built on a breadboard with all of its nonlinearities. The semiconductor models, the transformer and its associated leakage elements, and the peripheral elements are normally included. In this case, the time variable **t** is of utmost importance since it controls the overall circuit operation and performance, including semiconductor losses and ringing spikes which are due to parasitic elements. Because SMPS circuits usually operate at high frequencies and have response times on the order of milliseconds, analysis times may be very long. Furthermore, it is practically impossible to evaluate the AC transfer function of the simulated circuit due to the switch.

Average models do not contain the switching components. They contain a unique state equation which describes the average behavior of the system: in a switching system, a set of equations describe the circuit's electrical characteristics for the two stable positions of the switch/ (es), ON or OFF. The "state-space-averaging" technique consists of smoothing the discontinuity associated with the transitions of the switch/ (es) between these two states. The result is a set of continuous non-linear equations in which the state equation coefficients now depend upon the duty cycles **D** and **D′** (1-D). A linearization process will finally lead to a set of continuous linear equations. An in-depth description of these methods is contained in D. M. Mitchell's book, "DC-DC Switching Regulators Analysis", distributed by e/j BLOOM Associates (71147,3274).

The general simulation architecture

The key to understanding the simulation of SMPS with a SPICE simulator is to first experiment with very simple structures. Figure 1 shows the basic way to simulate an average voltage-mode Flyback converter with its associated components. As a starting point, simply draw a minimum

part count schematic: simple resistive load, output capacitor with its ESR, perfect transformer (XFMR symbol), no input filter, no error amplifier etc.

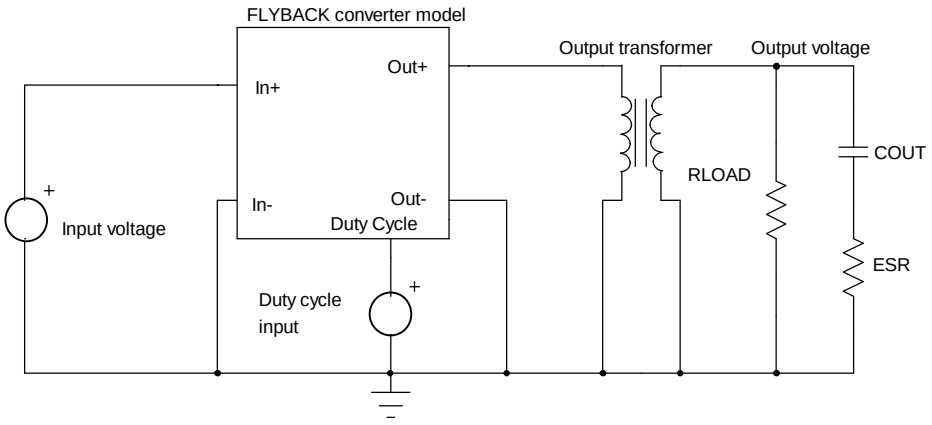


Figure 1

By clicking on the average Flyback model symbol or simply filling in the netlist file, the working parameters will be entered, i.e. the operating switching frequency, the value of the primary power coil, etc. Some recent models require the loop propagation delays or overall efficiency. The parameters for the remaining components are obvious, except for the duty cycle input source. This source will directly pilot the duty cycle of the selected model. By varying the source from 0 to 1V, the corresponding duty cycle will sweep between 0 and 100%. For the first simulation, without an error amplifier, you will have to adjust this source such that the output matches the desired value. This value corresponds to the DC operating point that SPICE needs for its calculations. The correct value can be determined incrementally or via the features in Intusoft's (San-Pedro, CA) IsSpice software. The Interactive Command Language (ICL), is a tremendously powerful language which has been primarily derived from the SPICE3 syntax and allows the designer to dynamically run SPICE commands without going back and forth from the schematic to the simulator. Below is a brief example of how the previous iteration process could be written:

```
while V(OUT)<=15                    ;while the voltage at node OUT is less than or equal to
15V
tran 1u 100u                        ;run a TRANSIENT analysis lasting 100us
alter @Vduty[dc]=@Vduty[dc]+1mV     ;increment the duty source by 1mV steps
print mean(V(OUT)) mean(@Vduty[dc]) ;print the output and the duty source average values
end
```

The SPICE simulator will compute the different values and refresh the output windows until the specified conditions are met. At this time, Vduty for the desired output value is known and can be reflected back to the schematic. In order to reduce execution time, and yield a more precise result, you could also run a DC sweep, although this method is less flexible.

Simulation trick: temporarily replace your large output capacitor with a small value in order to shorten the necessary transient time at every iteration. Small values require fewer switching cycles in order to reach the output target level.

The Pulse Width Modulator gain

In a voltage-controlled Flyback SMPS, the conduction time of the primary switch depends upon the DC voltage that is compared with the oscillator sawtooth, as shown in Figure 2:

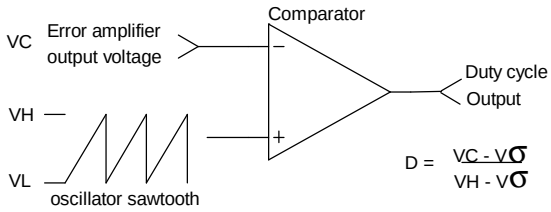


Figure 2

This circuit can be seen as a box which converts a DC voltage (the error amplifier voltage) into a duty cycle (D). The average models accept a 1 volt maximum duty cycle control voltage (D=100%). Generally, the IC's oscillator sawtooth can swing up to 3 or 4 volts, thus forcing the internal PWM stage to deliver the maximum duty cycle when the error amplifier reaches this value. To account for the 1 volt maximum input of our average models, the insertion of an attenuator with 1/(VH-Vσ) ratio after the error amplifier output is mandatory. For example, if the sawtooth amplitude of the integrated circuit we use is 2.5Vp-p, then the ratio will be: 1/2.5=0.4. In our simulation schematic, to account for the previous sawtooth peak-to-peak value, we would have to restrict the maximum output value of the error amplifier to 2.5 volts and limit the lower value to greater than VL. Figure 3 updates the schematic of Figure 1.

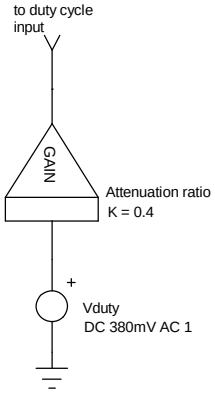


Figure 3

Performing AC simulations

We now have a functional open-loop system with the correct DC output value. The purpose of the next stage will be to sweep the duty cycle source around its DC steady-state level. This will give us the open-loop AC response of the circuit. The Vduty source keeps its DC statement to provide SPICE with a DC point, but the AC 1 command is added. Monitoring the AC output voltage yields the graph of Figure 4, which shows the control to output transfer function for a discontinuous Flyback converter.

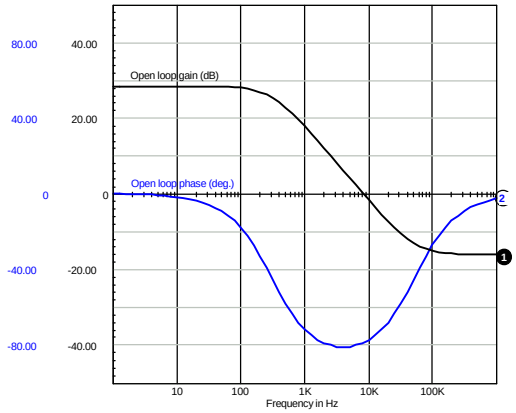
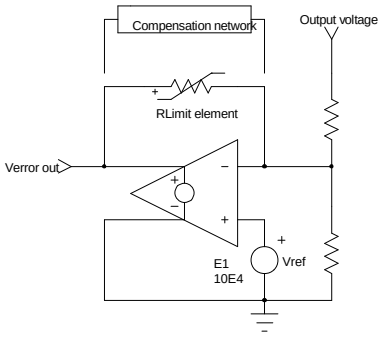


Figure 4

Adding the error amplifier

The error amplifier can be selected in function of various criteria: bandwidth, open-loop gain, etc. From a SPICE point of view, the simpler the model, the faster the simulation runs. The easiest method is to use a perfect amplifier like the one depicted in Figure 5a. This model is a simple voltage controlled source which amplifies the input voltage by the open loop gain. To overcome the problems associated with perfect sources, i.e. unrestrained output voltage, the action of a limiting element will confine the output voltage swing within a convenient range. This model is the simplest error amplifier model you can create. Figure 5b represents a transconductance type with its associated clipping network.



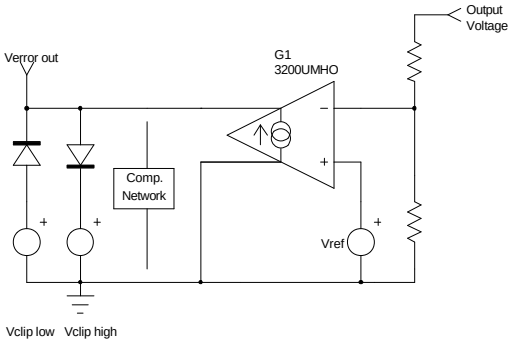


Figure 5a **Figure 5b**

To account for the characteristics of the error amplifier integrated in your real PWM controller, some components have to be added in order to tailor the response curve. The previous models do not really lend themselves to the addition of various internal pole and zero transfer functions.

Figure 5c shows another type of amplifier that will facilitate this task.

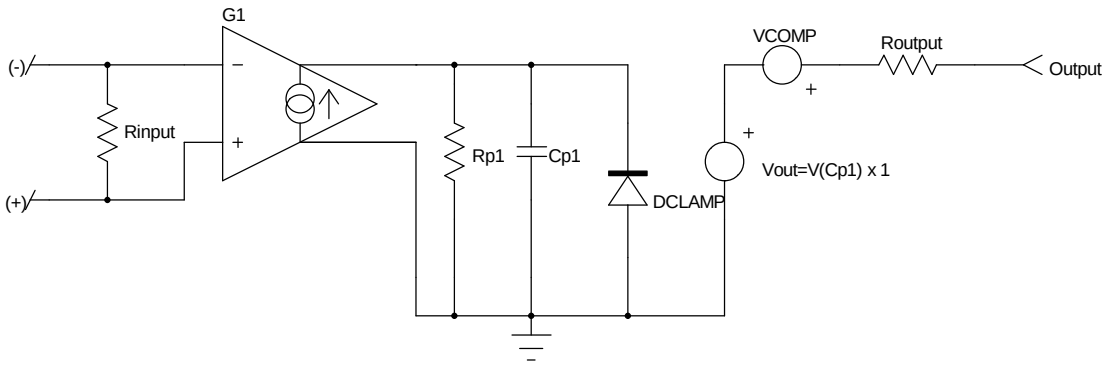


Figure 5c

This complete model associates a voltage controlled current source and a unity gain buffer. The first pole is modeled across Rp1 and Cp1, while other passive filter structures may be added between Cp1 and the unity gain buffer. The first stage output clipping is made via the diode DCLAMP and forces the output voltage of G1 to remain within the desired boundaries. Thus, the negative limit is the diode threshold voltage and the upper limit corresponds to the breakdown voltage of the diode. It can be adjusted by the IsSpice BV parameter in the diode model. In order to deliver an output voltage which matches the amplifier specifications, the VCOMP source will compensate the negative threshold of the diode, but also has to be reflected back to its BV value. In our example, the amplifier swings between 200mV and 5V with the following values: **.**MODEL DCLAMP D (BV=4.2V IBV=10mA) and VCOMP=680mV, as Figure 5d shows:

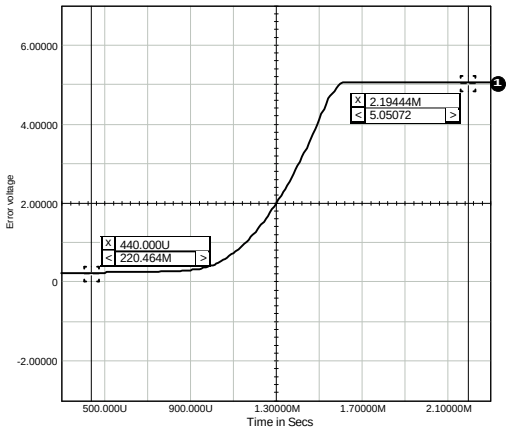


Figure 5d

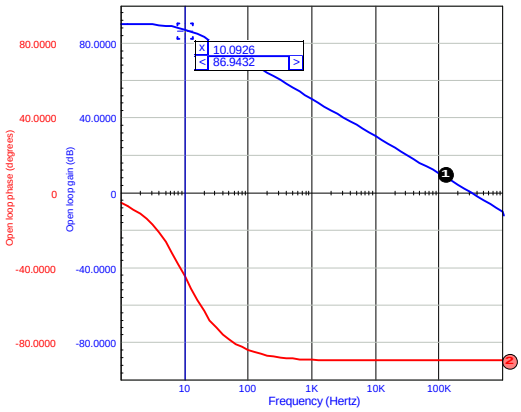


Figure 5e

The open loop gain is given by: AV_{OL} = G1*Rp1. With G1=100µMHOS and Rp1=316MΩ, we have an open loop gain of 90dB. The first pole is at 1/2πRp1.Cp1, which is 10Hz if Cp1=50.36pF. Figure 5e confirms these results.

Simulation trick: Figure 5f provides an alternative for connecting the reference voltage. It offers better transient behavior and simplifies the feedback network as a first approximation. Note that Vref now becomes -Vout, with $R_{ref} = R_i$.

The R_{ref} resistor in series with the VREF source does not play a role in the loop gain, as long as AOP is closed by R_f. This condition maintains a virtual ground at the negative input of AOP, and R_{ref} is in the loop gain calculation. But if you now remove R_f, or add a capacitor in series, the Vout/Output DC gain is no longer the open loop gain of AOP alone, but is multiplied by 0.5 ($R_{ref} = R_i$) because the negative pin is ½ Vout instead of zero.

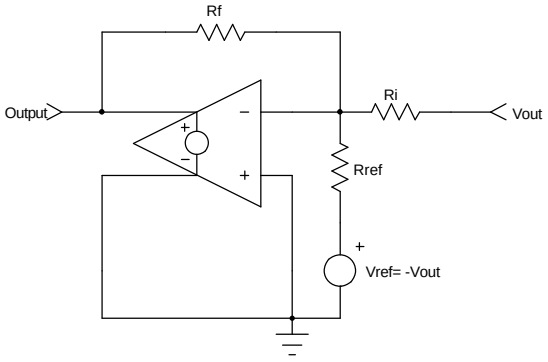


Figure 5f

Some SPICE editors not only propose the switching models of many PWM controllers, but also their standalone internal error amplifiers that can easily be incorporated in place of the previous simplified structures.

Opening a closed loop system

When the complete SMPS structure is drawn, it might be interesting to temporarily open the loop and perform AC simulations. The error amplifier can thus be isolated, and the designer has the ability to adjust the compensation network until the specifications are met. The fastest way to open the loop is to include an LC network as depicted in Figure 6. The inductive element maintains the DC error level such that the output stays at the required value, but stops any AC error signal that would close the loop. The C element permits an AC signal injection, thus allowing a normal AC sweep.

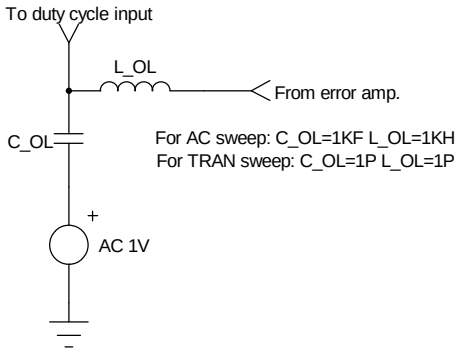


Figure 6

This method has the advantage of an automatic DC duty cycle adjustment, and allows you to quickly modify the output parameter without having to adjust the duty source.

Average simulation of the Flyback converter in discontinuous mode

Figure 7a shows a complete average Flyback converter made with Dr. Vincent Bello's models. These models use SPICE2 syntax and can therefore be run on any SPICE compatible engine.

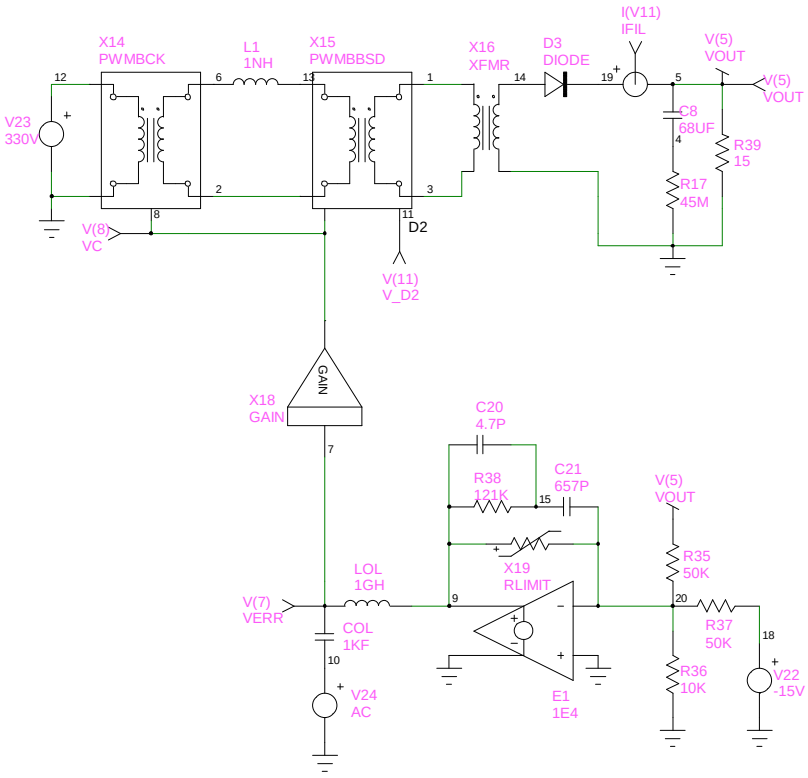


Figure 7a

In [3], Dr. Bello described the basic structure models (Buck, Boost ...) and showed how to create topologies such as Flyback and Forward converters. At this time, one model correspondeds to a particular Conduction Mode: Continuous (CCM) or Discontinuous (DCM). The Flyback converter operating in DCM is built with the PWMBCK (Buck) and the PWMBBSD (Discontinuous boost) as depicted in Figure 7a. The primary coil is simply shortened since it does not affect discontinuous operation in the average model. However, Dr. Bello states that despite state-space average technique results, keeping the inductor at its nominal value produces a second high-frequency pole and a RHP zero, as Vorperian demonstrated [4].

In the models we used here, PWMBBSD has to be modified such that it accounts for operating parameters. In our application (see parameters below) E2 will take the following value:

E2 25 0 1 2 1.25M ; E2 = 1/2*L*F_{SW}=T_{SW}/2*L

The SMPS drawn represents an off-line wall-adapter delivering 15V@1A. Its nominal characteristics and the corresponding pole-zero calculation are described below:

Operating parameters:

V_{out}=15V	I_{nom}=1A	R_{load}=15Ω	
V_{in}=330V	L_p=4mH	N_s/N_p = 0.05	
C_{out}=68µF	ESR=45mΩ	F_{sw}=100kHz	V_{ramp}=1.7Vpp

The iteration process gave a Vduty source of 581mV, which corresponds to a duty cycle of 34.2% (0.581/1.7)

G_{PWM} = 1/1.7 = -4.6dB
K = $2L_pF_{sw}$ / (R_{load} * $(N_s/N_p)^2$) = 0.1333
G_1= (V_{in} / √ K) * N_s/N_p = 45.19 = 33.1dB
$G_{Vout/Vduty}$= G_1(dB) + G_{PWM}(dB) = 28.5dB (26.6)
$G_{Vout/Vin}$= (D / √ K) * N_s/N_p = 0.0468 (-26.6dB for the open-loop DC audio susceptibility)
F_{P1} = 2 / 2π$C_{out}R_{load}$ = 312Hz
F_{z1} = 1 / 2 πC_{out}ESR = 52kHz

To verify the various gains, we open the loop and insert a DC source of 581mV, as previously shown in Figure 3. Then we ask SPICE to perform a .TF (Transfert Function) analysis:

.TF V(5) Vduty ; dV_{out}/dV_{duty} open loop gain
.TF V(5) Vin ; dV_{out}/dV_{in} open loop gain, audio susceptibility

Once computed, the results are placed in the output file. In our application, the .TF statements gave 26.49051 and 0.04544, respectively. The open-loop characteristics of this Flyback operating in DCM were already depicted in Figure 4.

If the amplifier error exhibits a gain A_{ErrAmp} , and in the absence of a divider network (Figure 5f), the new closed loop parameters can be expressed as:

dV_{out}/dV_{in}= ($G_{Vout/Vin}$) / (1 + $A_{ErrAmp}G_{Vout/Vduty}$) closed loop audio susceptibility
ε = Vref * [1 / (1 + $A_{ErrAmp}G_{Vout/Vduty}$)] static error

For instance, suppose that an error amplifier with a gain of 100 and a 15V reference voltage is used to close the previous SMPS. With the simulated parameters, the static error is evaluated at: 15*1 / (1 + 100*26.49051) = 5.66mV. The output voltage is then 14.99434V. If we now step the input voltage by 10V, the corresponding rise in output voltage will be:
10*0.04544 / (1 + 100*26.49051) = 171.5µV, which is 14.99451V. Figure 7b shows how SPICE reacts to this test.

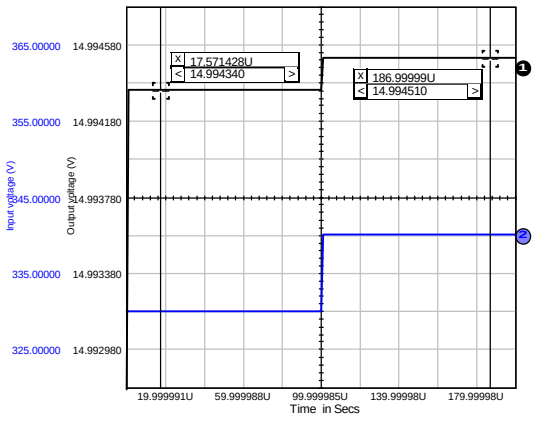


Figure 7b

Once all of the modifications are done, the designer can easily tailor the error amplifier so that the SMPS fulfills his target criteria. In our example, the compensation network gives a 21kHz bandwidth (Figure 7c).

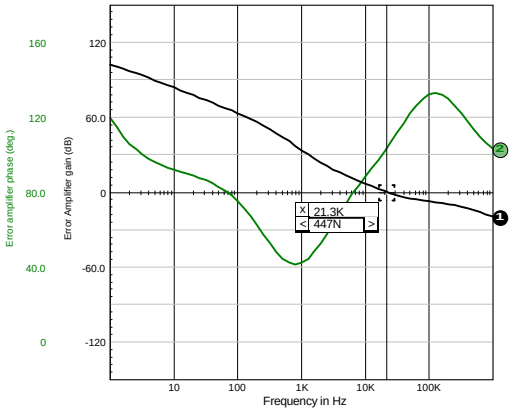


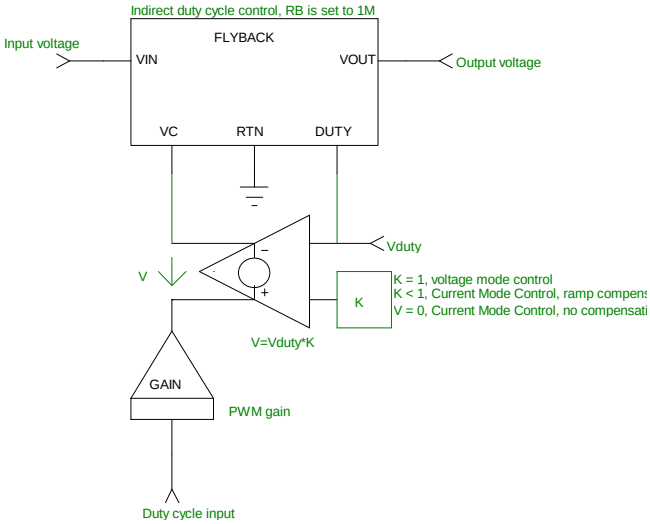
Figure 7c

New generation models

Intusoft has recently released a SPICE model library for Power Supply designers that includes new models that work in both DCM and CCM and can also be configured in current mode. The library also includes models for various PWM and PFC ICs. These SPICE3 compatible models have been developed by Steven Sandler of Analytical Engineering (Chandler, AZ) and are fully described in [5].

The models are represented by a single box in which the user enters the typical working parameters: Lp, F_{sw} etc. but also new parameters such as overall efficiency, propagation delay, and load resistance. By adding an external voltage source, you can configure the model the way you want to: voltage mode control, voltage mode control with feedforward, or current mode control with/without compensation ramp.

The Flyback model is the one of our main interests, and its symbol appears in Figure 8a with its associated parameters. The various operating modes are obtained by inserting an external voltage source in series with the VC input with the proper polarity, as shown in Figure 8a.



<u>Flyback parameters</u>:

L = primary coil, NC = current sense transformer turns ratio

NP = output transformer turns ratio; F = operating frequency, EFF = efficiency
RB = current sense resistor; TS = current loop propagation delay

Figure 8a

Figure 8b shows the same SMPS as the one we previously studied. The circuit is built with the Flyback model in direct duty cycle control, and the simplified error amplifier structure is replaced with an amplifier model like that which is shown in Figure 5c.

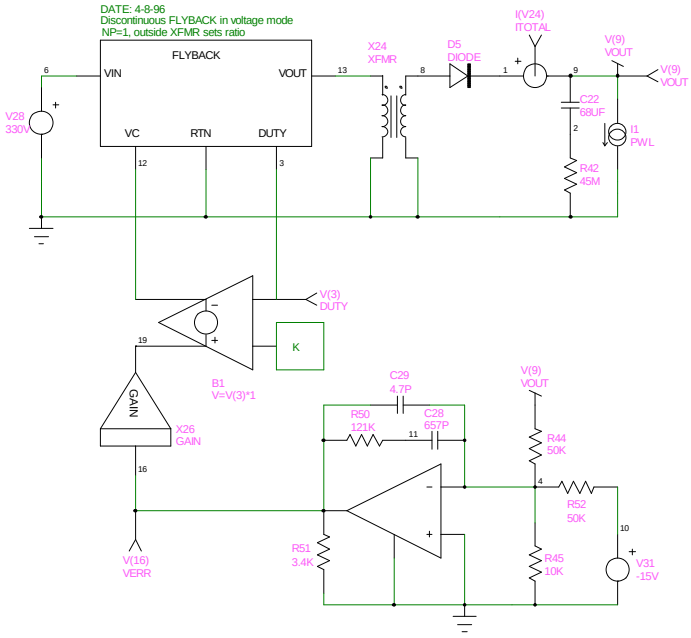


Figure 8b

The output is loaded by a current source whose purpose is to make the supply react to a sudden load increase, as shown in Figure 8c.

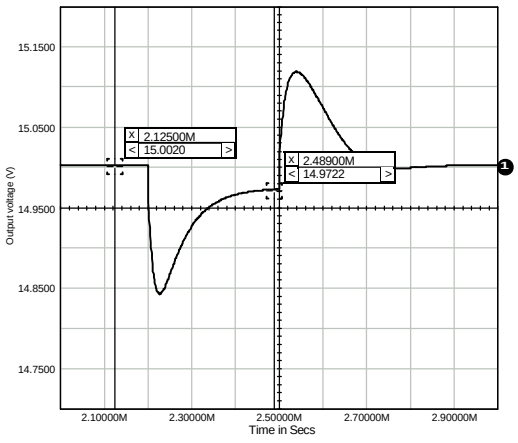


Figure 8c

At this stage, you can modify the error amplifier structure and modify the configuration until the SMPS behaves as required.

Current Mode Control SMPS

The Flyback model can be easily modified to toggle from one structure to another. Figure 9a shows the new arrangement of the current mode control without implementing any ramp compensation.

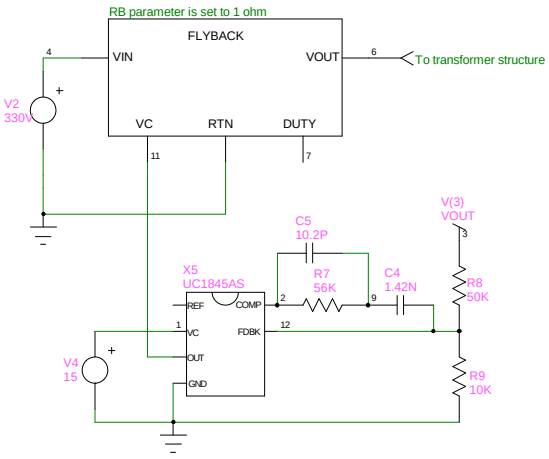


Figure 9a

In our application, the internal RB, the current sense element, is set to 1Ω. The compensation network has been slightly modified in order to account for the different gain values. The $G_{Vout/Vduty}$ gain now depends upon the current control factor (K) which is set by the sense resistor and, if present, by the internal current gain and the current sense transformer ratio. The error amplifier is replaced with the real UC3845 amplifier which is available as a single SPICE model. Its output is clipped to 1V and the output of the internal error amplifier goes through a diode before it is divided by 3, just as it is built in the real part. You may easily add a compensation ramp, as Figure 8a describes, with a simple voltage-controlled source and the appropriate coefficient.

One of the features of the Current Control Mode is its inherent feedforward capability. Figure 9b compares the response to an input step of the previous direct duty cycle SMPS and its Current Mode Control version. The **.**TF statement gives a $G_{Vout/Vin}$ of 0.0067, which is 17dB better than the equivalent direct duty cycle version.

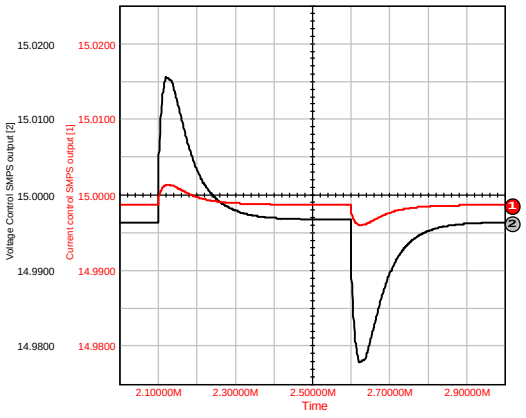


Figure 9b

Input impedance of the power supply

The input impedance has a direct impact on the overall stability when an EMI filter is connected in front of the supply. SPICE will help the designer to select an EMI structure without degrading the characteristics of the power supply. The DC value of the input impedance is easily calculated by: $Z_{in} = V^2_{in}\eta/P_{out}$. (For our 85% efficiency, 15W SMPS operating on a 330V source, the impedance is 6.17kΩ or 75.8dBΩ). Unfortunately, the input impedance is complex. It varies with the frequency and exhibits a negative peaking which is somewhat damped, depending on the SMPS

structure. The EMI filter is primarily an LC network. If this network is loaded by a negative resistor whose value perfectly compensates the ohmic losses of the coil, any excitation of the LC network will make it oscillate. Because of the closed loop system, the dynamic impedance, dV_{in}/dI_{in} is negative. To avoid the previous situation, the designer should keep the input impedance, Z_{in}, well above the filter's output impedance Z_{out}. Current Control Mode Power Supplies are less sensitive to the input impedance peaking. When used in conjunction with an EMI filter, these SMPS will be less sensitive to the negative resistance effect than their Voltage Mode counterparts. Figure 9c clearly shows the differences in the Z_{in} variations depending on the SMPS topology: Voltage Mode or Current Mode Control.

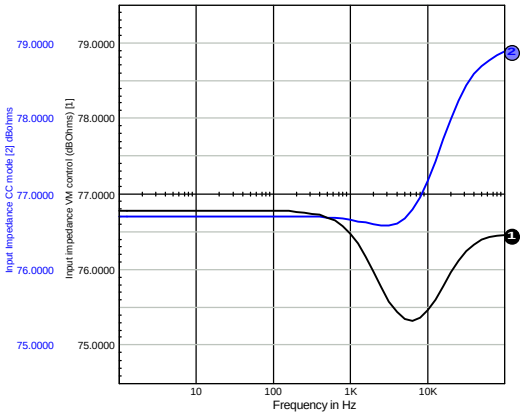


Figure 9c

Once the EMI filter is selected, an excitation stimulus on the input or the load will immediately reveal any parasitic resonance, thus inviting the designer to modify its calculations.

The Flyback converter in continuous conduction mode

In [6], D. Caldwell showed in practical terms how to implement the PWM switch theory as described by V. Vorperian [4], but, unfortunately, did not give any application examples. The Unicon model is written in SPICE2 syntax and thus permits its use on various compatible platforms. It operates in both DCM and CCM. Figure 10 shows a continuous power supply which uses the Caldwell model. The SMPS operates in continuous mode and delivers 12V to a 2.4Ω resistive load. As the author stated in his article, you need to edit the UNICON netlist and modify the EDIS generator in order to account for the operating parameters: for a 66µH coil associated with a 80kHz operating frequency, the last EDIS parameter equals 0.0947*(T/2L).

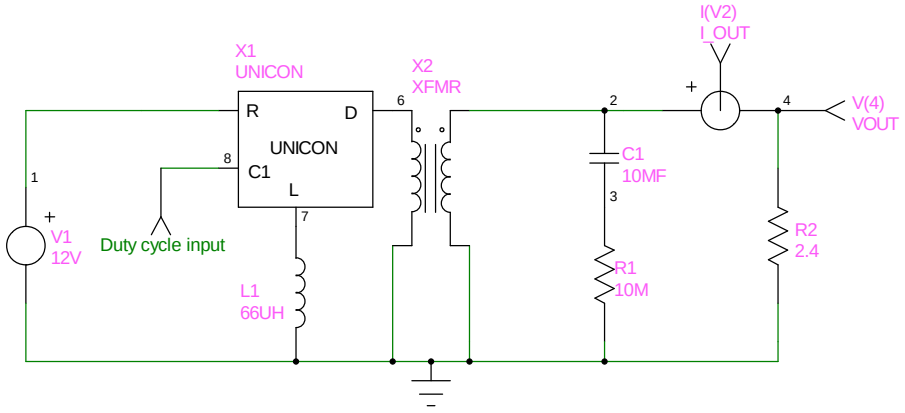


Figure 10

The Flyback operating in the continuous voltage mode is always harder to stabilize because of its second order behavior, and also because of the presence of a Right Half-Plane (RHP) zero. The RHP zero moves with the operating parameters and the designer is forced to roll-off the gain so that

the SMPS stays stable within its operating range. Once again, SPICE will ease the designer's task by providing all of the necessary investigation tools to cover the numerous situations encountered by the design in its future life.

Figure 11 depicts another Flyback converter structure, using a model introduced by Lloyd Dixon in [7]. The model was originally written in PSpice syntax (Microsim, Irvine, CA), but the use of arbitrary SPICE3 B sources can easily accomplish the same functions, as we'll describe later. The model works in both operating modes, CCM and DCM. In DCM, the model naturally accounts for the high-frequency Vorperian's pole and RHP zero. The compensation of the error amplifier takes into account the presence of the low frequency pole and zeros, as described below:

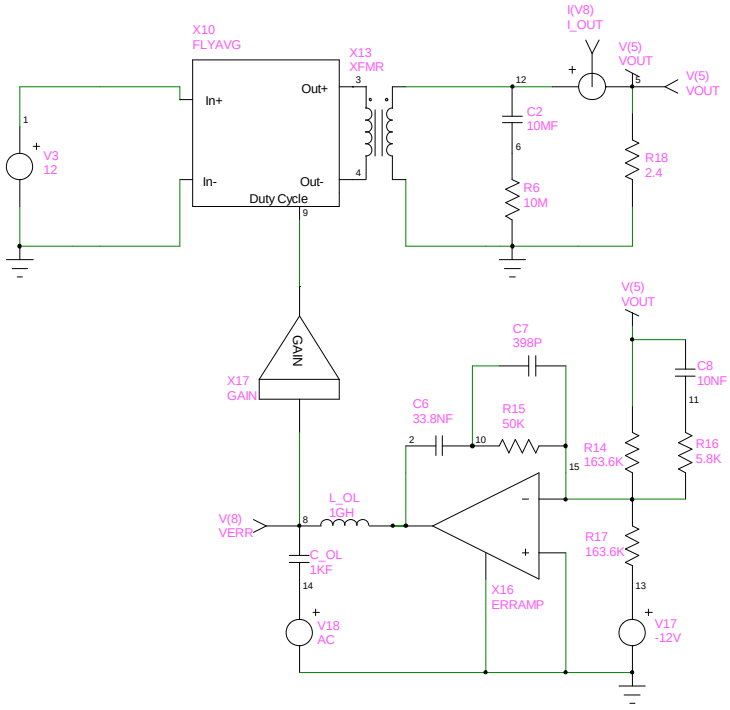


Figure 11

Operating parameters:

V_{out}=12V	I_{nom}=5A	R_{load}=2.4Ω	
V_{in}=12V	L_p=66µH	N_s/N_p = 1.1	
C_{out}=10mF	ESR=10mΩ	F_{sw}=80kHz	V_{ramp}=2.5V_{pp}

Reflected output voltage at the primary: $V_r = V_{out} / (N_s/N_p) = 10.91V$, neglecting the diode's voltage drop

$D_{nom} = V_r / (V_r + V_{in}) = 0.476$
$L_e = L_p / (1-D_{nom})^2 = 240.4\mu H$
$G_{PWM} = 1 / 2.5 = -7.96dB$
$G_1(dB) = V_{in} / (1-D_{nom})^2 = 32.8dB$
$G_2(dB) = 20LOG\ (N_s/N_p) = 0.83dB$
$G_{Vout/Vduty} = G_1(dB) + G_{PWM}(dB) + G_2(dB) = 25.7dB$
$G_{Vout/Vin} = D_{nom} / (1 - D_{nom})*N_s/N_p = V_o/V_{in} = 1 = 0dB$
$F_{P1} = 1 / 2\pi N_s/N_p\sqrt{C_{out}L_e} = 93.31Hz$
$F_{z1} = 1 / 2\pi ESR*C_{out} = 1.591kHz$
$F_{z2} = R_{load} / [(N_s/N_p)^2*D_{nom}L_e2\pi] = 2.758kHz$ (Right Half-Plane zero)

You could also use the V. Bello models, as already described in Figure 7a. To make the converter operate in continuous conduction mode, simply replace the PWMBBSD model with the

PWMBST model, without modifying its internal node list. This block is also fully documented in the reference papers [3]. The coil is set to its nominal value (66µH) and you can immediately run an AC analysis to obtain the plot of Figure 12. Nevertheless, the error amplifier compensation network which is shown in Figure 7a is no longer valid to stabilize the continuous SMPS. The one which is shown in Figure 11 represents a possible solution.

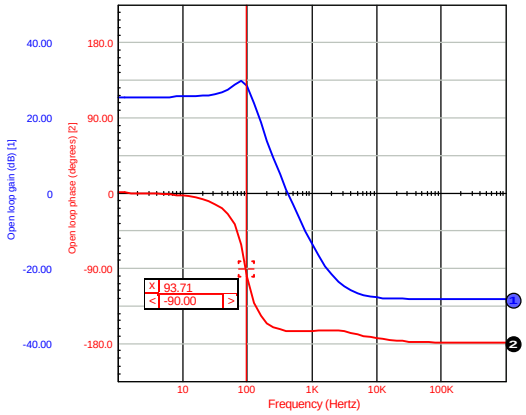


Figure 12

The -90° point corresponds to the -3dB cutoff of the second order system. Note that this value, and also the open-loop gain, are very close to the ones theoretically calculated. At F_{z1}, the slope becomes -1 with a boost in the phase plot. F_{z2} starts to act and because of its position in the right half plane, it induces a phase lag. The slope is now 0. This graphic immediately shows you where the various poles and zeros are located, and, by varying some key parameters, you can follow their respective displacements. The compensation network which has been calculated using the worst case conditions then becomes more straightforward.

The closed loop audio susceptibility is easily evaluated by decreasing C_OL and L_OL to 1pF and by adding the AC 1 statement to the input source. Figure 13 shows how the supply behaves.

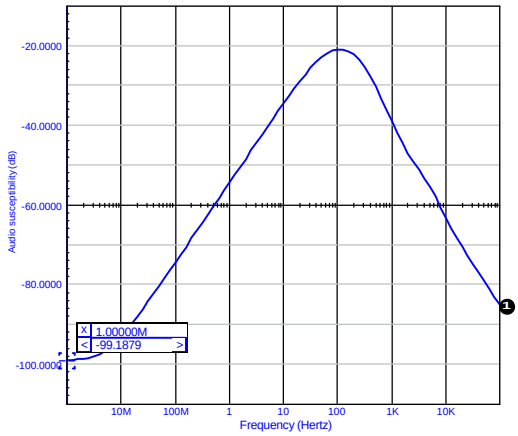


Figure 13

The open loop gain obtained by the **.**TF statement, $G_{Vin/Vout}$ and $G_{Vout/Vduty}$, respectively, is 0.9983 and 18.503. The AOP of Figure 11 exhibits an open loop gain of 10k. But, as we previously stated, in the absence of a feedback resistor, the Vout/Verr gain becomes 5k. The DC audio closed loop susceptibility is then: 20LOG[0.9983 / (1 + 18.503*5000)] = -99.3dB

Limitations inherent to the continuous voltage mode

The error amplifier structure depicted in Figure 11 severely impairs the time response of the power supply in the presence of large output variations. The elements responsible for this behavior are the C7 and C8 capacitors which charge to large transient values when the error amplifier's output is

pushed to its maximum. This phenomenon is described in details in [9]. To highlight this problem and eventually compensate it, simply replace the load by a PWL current source that simulates a large load step. Figure 14 represents the simulation result of the error amplifier's output and indicates the amount of time which is required in order to properly recover the output transient.

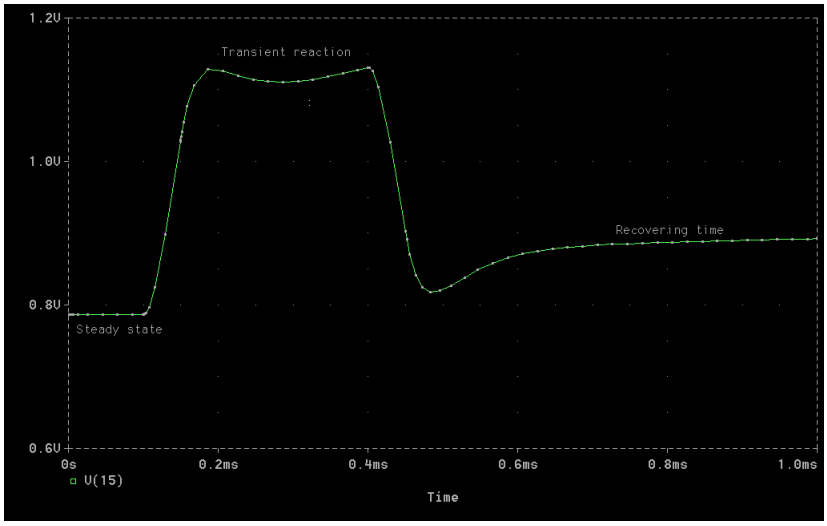


Figure 14

Using the models with different platforms

The use of a model can be extended to various SPICE compatible platforms as long as its syntax conforms to the Berkeley definition. For instance, the simple G, E or complex polynomial sources (POLY) allow the model to be used with different simulators. But if the designer adopts a proprietary syntax, he naturally reduces the implementation of his models among the remaining systems. Lloyd Dixon's model in [7] uses PSpice syntax to clamp the output voltage of some internal sources. This syntax is not SPICE3 compatible. If you would like to run the model with Intusoft's IsSpice or Cadence's Analog WorkBench (San-Jose, CA), you'll need to modify the syntax. One easy solution lies in working with arbitrary sources or B elements, since they accept in-line equations or implement If-Then-Else structures. As a first step, let's look at the following PSpice lines as they are written in Dixon's Flyavg model. The first is intended to limit the output variations of a generator within users-defined boundaries, and the second sets the value of the current generator:

```
ED2     12 0     TABLE {V(11A)-V(11)}  100M,100M 1,1          ; PSpice voltage source
G0       4 3     VALUE = {V(9,8)*1000*V(12)/(V(11)+V(12))}    ; PSpice current source
```

If you try to run these lines using the previously referenced simulators, the internal parser will generate an error. The ED2 generator produces a voltage equal to the difference between nodes 11A and 11, but its output is clipped between 100MV and 1V. For IsSpice and AWB, these lines will look like this:

```
B_ED2 12 0 V = V(11A,11) < 100MV ? 100M : V(11A,11) > 1 ? 1 : V(11A,11)          ; IsSpice
B_ED2 12 0 V = IF ( V(11A,11) < 1, IF (V(11A,11) < 100M, 100M, V(11A,11)),1)     ; AWB
```

The Boolean style helps you to understand these lines: If the first condition V(11A,11) < 100MV is true, Then ED2=100MV, If the second condition V(11A,11) > 1V is true Then ED2 = 1V, Else (if any of the two previous conditions is met) ED2 = V(11A,11).

The G0 current generator can also be simply written as:

```
B_G0 4 3 I = V(9,8)*1000*V(12)/(V(11)+V(12))     ; IsSpice and AWB
```

or, for a voltage source:

```
B_ED 4 3 V= V(9,8)*500*V(13)                     ; IsSpice and AWB
```

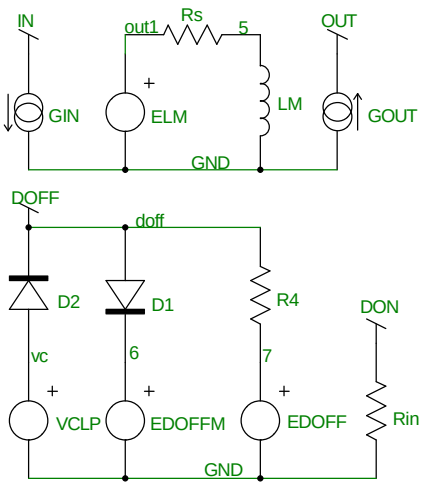
Microsim's PSpice also has If-Then-Else conditions, and thus allows you to write logical expressions. For instance, suppose you want to build a perfect comparator whose output is the B1 voltage source, then the following lines illustrate how to make it with through the different syntax:

```
B1      OUT GND V = V(PLUS) > V(MINUS) ? 5V : 10MV                  ; IsSpice (C syntax)
B1      OUT GND V= IF ( V(PLUS) > V(MINUS), 5, 10M )                ; AWB
E_B1    OUT GND VALUE = { IF ( V(PLUS) > V(MINUS), 5V, 10MV ) }     ; PSpice
```

Because of their perfect behavior, the B elements used in comparison functions often require a small RC circuit as an output interface to slow down their transitions. Fixed resistors between the inputs and ground may also be necessary in order to provide the simulator with a DC path in the presence of infinite Pspice input impedances. IsSpice implements the statement .OPTIONS RSHUNT=100MEG, which adds a DC path of 100MEGΩ to ground for all the nodes in the simulated circuit.

Modeling the Flyback converter, other solutions

Professor Sam Ben-Yaakov, from the Ben-Gurion University of the Negev (Israel), has developed a range of models for simulating numerous converter structures [10]. The Flyback model he created is of great interest for the designer since it works for both continuous and discontinuous modes. Another nice feature lies in its simplicity, making the simplifies the conversion from one simulator to another. Figure 15 shows its internal connections and associated sources. The full model is described in Listing 1.



GIN = I(LM)*V(DON)/(V(DON)+V(DOFF))
ELM = V(IN)*V(DON)-V(OUT)*V(DOFF)/N
GOUT = I(LM)*V(DOFF)/N/(V(DON)+V(DOFF))
EDOFFM = 1-V(DON)-9M
EDOFF = 2*I(LM)*FSW*LM/V(DON)/V(IN)-V(DON)

Figure 15

Listing 1 describes a full functional netlist of the discontinuous converter of Figure 7a. The model accounts for the high frequency pole and the RHP zero highlighted by Dr. Vorperian's work. These combined actions can be seen in Figure 16. These points are well above the switching frequency and, most of the time, they can be neglected by the designer. You should always keep in mind that any reference to and/or discussion of poles or zeros above 1/2 the switching frequency is purely fictitious. The poles and zeros in question (other than the first pole and ESR zero) will always shift toward high frequencies at which the average model does not hold. The Nyquist sampling theorem restricts our ability to deal with cases in which the modulation signal is above 1/2 the

sampling (switching) frequency. Needless to say, from the engineering point of view, that the frequency response above 1/3 of the switching frequency is irrelevant.

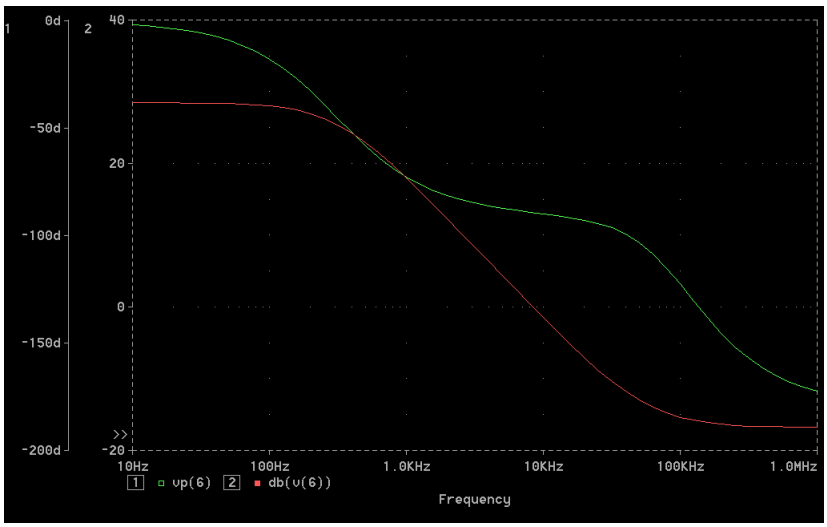


Figure 16

If we take the operating parameters of the first discontinuous Flyback converter example, we can calculate the values of the VORPERIAN's pole and zero, as described in his paper [4]:

$Sz_2 = R_f/M*(1 + M)*L_p$ Right Half-Plane Zero
$Sp_2 = 2F_{sw}*[(1/D) / (1 + 1/M)]^2$ Second High-Frequency Pole, D = 0.33
$R_f = R_{load}/(N_s/N_p)^2 = 6k\Omega$ Reflected load to the transformer's primary
$M = V_{out}/(N_s/N_p)/V_{in} = 0.909$ Transfer Ratio
The numerical application leads to: Fz_2 = 137.6kHz and Fp_2 = 66.3kHz.

If you do not want the model to account for the high-frequency pole and zero, you can, in discontinuous conduction mode, decrease the LM coil between nodes 5 and 8 to 1nH. You will then obtain a phase curve which is similar to the one in Figure 4.

Primary regulated Flyback converters

The primary regulation is a feedback method in which the output level is sensed via an auxiliary winding, thus avoiding all galvanic isolation related problems. If the average models cannot highlight the regulation defaults associated with leakage inductances, they may ease your work when you tackle the stability discussion. That is to say, when multiple outputs are implemented, all of the output networks (capacitors, loads etc.) have to be reflected back to the regulated winding with the corresponding turns ratios. Figure 17 shows how to modify the previous structures in order to implement primary regulation and perform fast and efficient AC analysis.

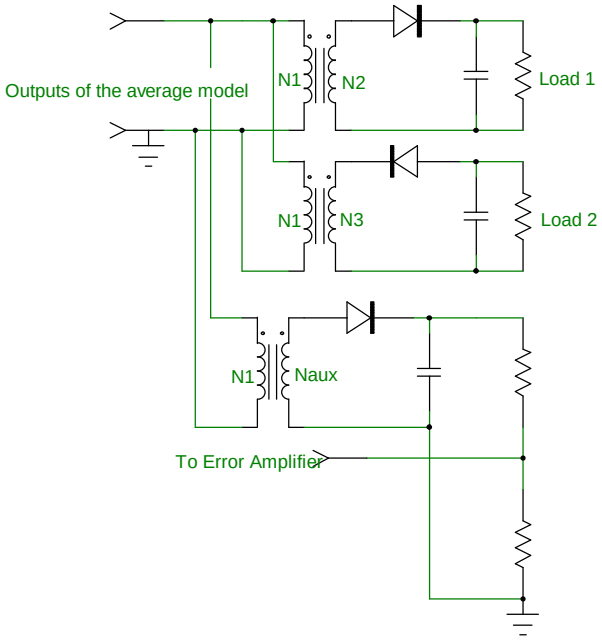


Figure 17

Conclusion

The lack of comprehensive articles upon the subject has made the SPICE approach a difficult stage for SMPS designers who are not used to the simulation philosophy. This article presents a step-by-step method to implement the available models for simulating your own Flyback structures on a SPICE platform. The proprietary libraries and the public domain models will allow you to easily simulate other kinds of topologies such as Buck or Forward converters. Power Factor Correction simulations with Boost structures may also be accomplished, as demonstrated in [3], [5], and [7].

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Listing 1: Complete discontinuous Flyback converter with Sam Ben-Yaakov's model

```
****** SAM BEN-YAAKOV'S FLYBACK MODEL *******
.SUBCKT FLYBACK DON IN OUT GND
.PARAM FS=100K                  ; Switching frequency
.PARAM L=4M                     ; Primary coil
.PARAM N=1                      ; Internal transformer
GIN IN GND VALUE = { I(VLM)*V(DON)/(V(DON)+V(DOFF)) }
ELM OUT1 GND VALUE = { V(IN)*V(DON)-V(OUT)*V(DOFF)/{N} }
RM OUT1 5 1M
LM 5 8 {L}
VLM 8 GND
GOUT GND OUT VALUE = { I(VLM)*V(DOFF)/{N}/(V(DON)+V(DOFF)) }
VCLP VC 0 9M
D2 VC DOFF DBREAK
D1 DOFF 6 DBREAK
R4 DOFF 7 10
EDOFFM 6 GND VALUE = { 1-V(DON)-9M }
EDOFF 7 GND VALUE = { 2*I(VLM)*{FS}*{L}/V(DON)/V(IN)-V(DON) }
.MODEL DBREAK D (TT=1N CJO=10P N=0.01)
.ENDS FLYBACK
***** Perfect Transformer model ******
.SUBCKT TRANSFORMER 1 2 3 4
RP 1 2 1MEG
E 5 4 1 2 0.05
F 1 2 VM 0.05
RS 6 3 1U
VM 5 6
.ENDS TRANSFORMER
***** Error Amp. model ******
.SUBCKT ERRAMP 20 8  3  21
*                       +  - OUT GND
RIN 20 8 8MEG
CP1 11 21 16.8P
E1 5 21 11 21 1
R9 5 2 5
D14 2 13 DMOD
ISINK 13 21 150U
Q1 21 13 16 QPMOD
ISOURCE 7 3 500U
D12 3 7 DMOD
D15 21 11 DCLAMP
G1 21 11 20 8 100U
V1 7 21 2.5
V4 3 16 80M
RP1 11 21 316MEG
.MODEL QPMOD PNP
.MODEL DCLAMP D (RS=10 BV=2.8 IBV=0.01 TT=1N)
.MODEL DMOD D
.ENDS ERRAMP
**** PWM modulator Gain Model ****
.SUBCKT PWMGAIN 1 2
E1 2 0 1 0 0.5882
.ENDS PWMGAIN
**** PSpice Sam BEN-YAAKOV's model in Discontinuous mode ****
.TRAN 1U 1000US
.AC DEC 10 10HZ 1MEG
.PRINT AC  V(6)  VP(6)  V(13)  VP(13)
.PRINT TRAN  V(6)  V(13)
.PROBE
R1 4 0 45M                      ; Output Capacitor's ESR
C1 6 4 68U                      ; Output Capacitor
X8 11 1 5 0 FLYBACK             ; Sam BEN-YAAKOV's model
X9 5 0 6 0 TRANSFORMER          ; Output transformer
R8 6 8 50K
R9 8 0 10K
X11 2 11 PWMGAIN                ; PWM modulator gain
X12 0 8 13 0 ERRAMP             ; Error amplifier
V6 9 0 -15V                     ; Output reference voltage
R10 13 10 121K                  ; Erramp Compensation network
C5 10 8 657P                    ; Erramp Compensation network
C6 8 13 4.7P                    ; Erramp Compensation network
R12 9 8 50K
L2 2 13 1GH                     ; Open loop coil, 1P for .TRAN, 1GH for .AC
C7 2 3 1KF                      ; Open loop capacitor, 1P for .TRAN 1kF for .AC
V7 3 0 AC 1                     ; AC stimulus
* I1 6 0 PWL 0 100M 100U 100M 101U 1A 500U 1A 501U 100M
*                               ; Output step response for .TRAN run
RL 6 0 15                       ; Nominal load for .AC run
V1 1 0 330                      ; Input voltage
.END
```