A Tutorial Introduction to Simulating Current Mode Power Stages

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SPICE simulation of Current Mode Control (CMC) switch Mode Power Supplies (SMPS) is certainly not a new topic. A lot of people have contributed to make this domain affordable to the design engineer and nowadays EDA packages are shipped with comprehensive dedicated libraries. However, in lack of a tutorial documentation, the choice and the implementation of the models is not always obvious to the novice designer. This article will detail the utilization of 90's models developed around the PWM switch model and more recent ones included in the new INTUSOFT's IsSpice4 SMPS library package (San-Pedro, CA).

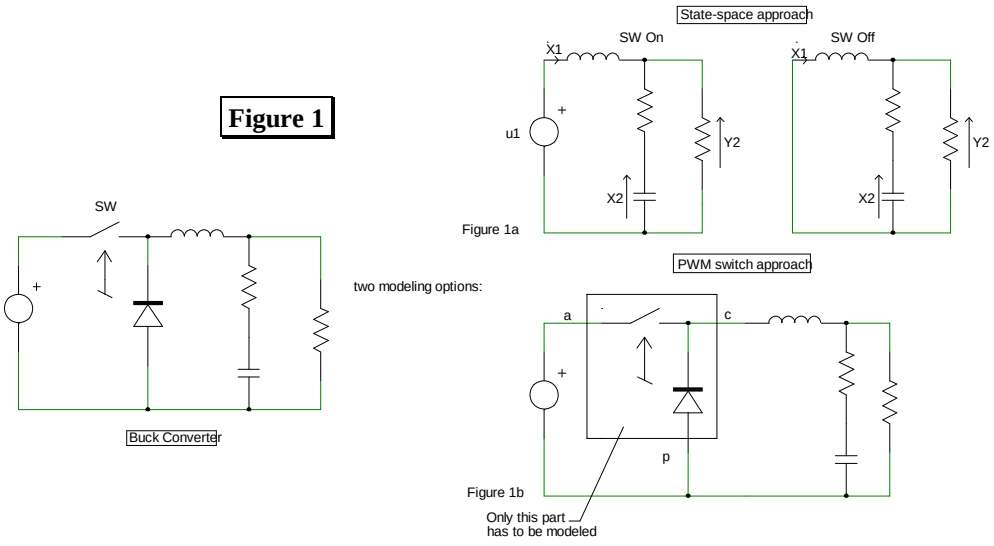
What kind of model do I need?

Depending on the analysis to be carried on, several choices are offered to the designer. The first one is called a Small-Signal Model (SSM). It assumes that the variations of concern (e.g. output or input voltages) are small around a steady-state DC operating point. In this case, second-order AC cross-products can be neglected and the model is linear around its operating point. The SSM is then usually employed for harmonic simulations where the AC transfer functions are of interest. Do not use a SSM to simulate a 100% transient load span, the result would be wrong since AC cross-products could no longer be negligible. Some SSM models can find their DC point alone, some not and the operating point must then be fed by the designer.

Vincent BELLO has been the first in the 80's to port MIDDLEBROOK's non-linear state-space average models to the SPICE domain [1]. In BELLO's models, the previous AC terms were no longer neglected but rather dynamically multiplied by some *POLY* SPICE2 statements. Large-signal variations could then be simulated and allowed the user to visualize the effects of a 0 to 100% duty-cycle sweep. These large-signal models (LSM) are best suited for TRANSIENT runs.

Modeling SMPS, two distinct approaches

There are two ways to model a SMPS system. The first one is the well known state-space averaging (SSA) method introduced by R. D. MIDDLEBROOK in 1976 [2]. Without describing the process once more, one can state that SSA models the converter in its entire electrical form, as shown in **figure 1a** for a BUCK. In other words, the SSA process is carried over all the elements of the converter, including various in/out passive components. Depending on the converter structure, the process can be very long and complicated .



In 1986, Larry MEARES and Vatché VORPERIAN, from Virginia Polytechnic Institute (VPEC), developed the concept of the PWM switch model [3, 3a]. VORPERIAN wondered why not simply model the power switch alone, and then insert an equivalent model into the converter schematic, exactly the same way it is done when studying the transfer function of a bipolar amplifier (**figure 1b**). With his method, VORPERIAN demonstrated among other results, that the flyback converter operating in discontinuous conduction mode (DCM) was still a second order system, affected by a high-frequency RHP zero.

Since its introduction, the PWM Switch has not been the object of many publications in the specialized press and some designers might think that its use is only reserved to modeling experts. Because its implementation is easy and powerful, we will go through a quick example, but without entering into the details of its electrical origins.

Calculating a transfer function with the PWM switch

The PWM switch model operating in Continuous Conduction Mode (CCM) is presented in **figure 2a** and can be split into an AC and a DC part. Isolating one part and applying it to the converter under study, gives the designer an immediate insight on how the converter performs in the domain of concern. Reference [3]'s BOOST example appears in **figure 2b** that shows how to properly include the PWM model. If we first consider the DC operation, Lf shorted and Cf open, **figure 2c** appears (re = R // rCf and D'=1-D).

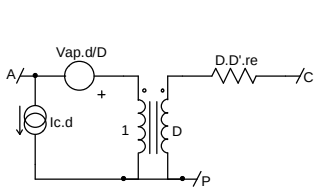


Figure 2a

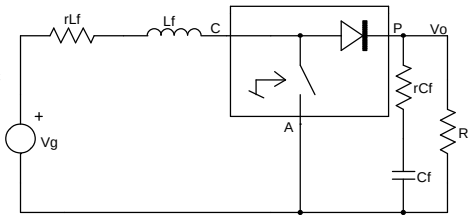


Figure 2b

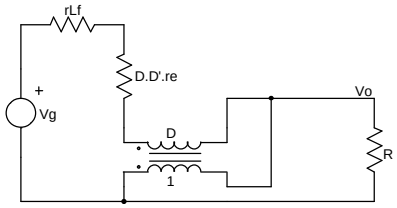


Figure 2c

There are different approaches to solve this kind of circuit where the transformer is not commonly wired: the classical brute force, using nodal and loop equations or the soft approach that will consist to transform the schematics until a well known structure is found. Generally speaking, the first method usually leads to correct but abstruse results in which the action of a component inside the considered function is not obvious. Inversely, the soft method produces so-called low entropy expressions [4] and yields insight into the circuit under study.

Let us adopt the second method, thus redrawing a simplified version of figure 2c, as depicted in **figure 3a**. We first mark the currents, keeping in mind that a current entering a winding by a dot leaves the coupled winding by the other dot, <u>in the same direction</u>.

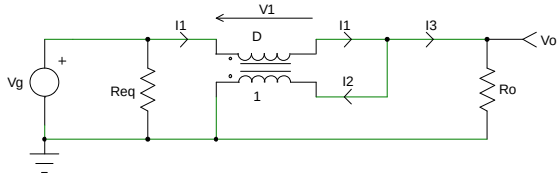


Figure 3a

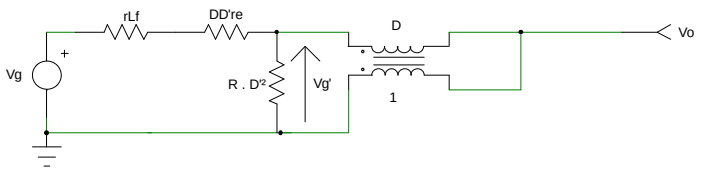


Figure 3b

The Vo/Vg transfer function is easily obtained after a few lines:

Vg - V1 = Vo
V1 = -Vo . D
Vg + Vo . D = Vo
Vg = Vo - Vo . D so Vo/Vg = 1 / (1-D) or **<u>Vo/Vg = 1/D'</u>** (1)

The input impedance, or the way Ro is reflected across Vg (Req), is also simple to derive:

N1.I1 = N2.I2. Since I1 = Vg/Req, it is possible to write:
N1 . Vg/Req = N2 . I2. From KIRCHHOFF's law, I2 = I1 - I3, with I3 = Vo/Ro
By definition, N1=D et N2=1
D . Vg/Req = Vg/Req - Vo/Ro
D . Vg/Req = (Vg . Ro - Req . Vo) / (Req . Ro). Simplifying by Req :
D. Vg = Vg - (Req . Vo)/Ro
Vg / Vo . (1 - D) = Req/Ro. From [1], Vg/Vo = 1-D, so: **<u>Req = Ro . D'²</u>** (2)

The I3/I1 ratio is important to feed the model with its DC operating points, as we will see later on. If Pin=Po, one can write: Vg. I1 = Vo . I3, so I1/I3 = Vo / Vg = 1 / D'. Back to VORPERIAN's model of figure 2b, **Ic = -I1 = - Io / D'**.

With these simple formulas, **figure 3b** represents our DC BOOST where Ro has been reflected according to equation (2). We are in presence of a simple resistive divider whose output Vg' undergoes a 1/D' multiplier ratio (1). Thus, the DC Vo/Vg transfer function is really straightforward. So, after

factoring the R.D'² term: $$\frac{Vo}{Vg}=\frac{1}{D'}\cdot\frac{1}{1+\frac{rLf}{D'^2\cdot R}+\frac{re\cdot D}{R\cdot D'}}=M \qquad (3)$$

The AC open-loop line to output transfer function will use the previous results to transform **figure 4a** to **figure 4b**'s drawing, where all the output elements (rCf and Cf) have been reflected to the other side of the transformer.

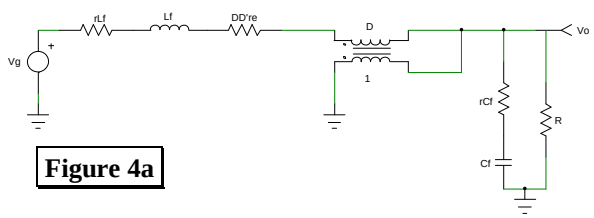


Figure 4a

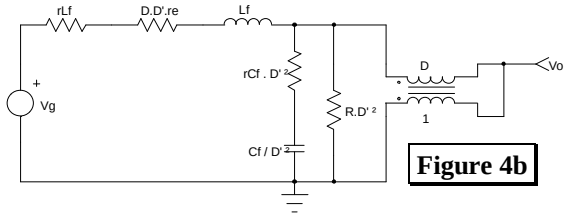


Figure 4b

Figure 4b unveils a classical LC filter affected by its parasitic elements, once again followed by a 1/D' multiplier. Since we want to obtain the Vo/Vg transfer function but also the Zin Zout parameters of this circuit, a good method is to use matrix algebra. Matrix algebra is well suited for numerical computations on a computer and SPICE makes an extensive use of it. It is true that the symbolic answer given by a transfer matrix does not give the designer much insight of the circuit's operation. But one remarkable point is that once you found the matrix coefficients, the resulting transfer matrix contains, in one shot, all the parameters of interest (**figure 5b**). Further, if matrixes require a constant attention when do you manipulate them by hand, it becomes a child play when you use some mathematics programs such as Mathsoft's MathCAD (Cambridge, MA).

To solve figure 4b's problem, we draw a simplified schematic of the LC filter (**figure 5a**) where we put state and output variables.

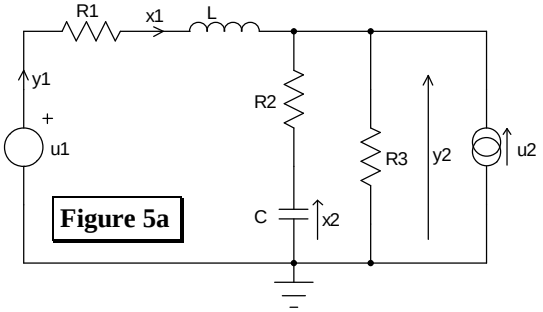


Figure 5a

$$T(s)=\begin{bmatrix}\frac{Y1(s)}{U1(s)} & \frac{Y1(s)}{U2(s)}\\ \frac{Y2(s)}{U1(s)} & \frac{Y2(s)}{U2(s)}\end{bmatrix}$$

$T_{1,1}$ = Zin

$T_{2,1}$ = Vo/Vg

$T_{2,2}$ = Zout

Figure 5b

The generalized transfer function of a n^{th} order linear passive system is: $M(s) = [M\ (sI-A)^{-1}\ B + N]$, where A and M are the state coefficient matrixes, B and N the source coefficient matrixes [5]. The steps will be to write the state and output equations, ordered as follows:

State equations

$$x1=-\frac{1}{L}\cdot\left[R1+\frac{R2\cdot R3}{(R2+R3)}\right]\cdot x1+\frac{1}{L}\cdot\left(\frac{R2}{R2+R3}-1\right)\cdot x2+\frac{1}{L}\cdot u1-\frac{1}{L}\cdot\frac{R2\cdot R3}{R2+R3}\cdot u2$$

$$x2=\frac{R3}{(R2+R3)\cdot C}\cdot x1-\frac{1}{C\cdot(R2+R3)}\cdot x2-\frac{R3}{C\cdot(R2+R3)}\cdot u2$$

Output equations

$Y1 = x1$

$$Y2 = x1 \cdot R3 \cdot \left(1 - \frac{R3}{R2 + R3}\right) + \frac{R3}{R2 + R3} \cdot x2 + u2 \cdot R3 \cdot \left(1 - \frac{R3}{R2 + R3}\right)$$

The final results delivered by MathCAD are in a clear ordered form. Vo/Vg ratio is extracted from figure 5b's matrix transfer, T_{21}:

$$\frac{Vo}{Vg} = \frac{1}{D'} \cdot \frac{R3}{R1 + R3} \cdot \frac{1 + s \cdot C \cdot R2}{s^2 \cdot L \cdot C \cdot \left(\frac{R3 + R2}{R1 + R3}\right) + \left[s \cdot \frac{L + C \cdot (R2 \cdot R3 + R3 \cdot R1 + R1 \cdot R2)}{R1 + R3}\right] + 1}$$

After replacing by the elements by figure 4b's values and putting the equation into a second order form, we extract the first zero s_{z1} and the tuning frequency ω_o:

$\omega_{z1} = 1 / R2.C = 1 / rCf$. Cf

$s^2.L.C.(R2+R3)/R1+R3 = s^2/\omega_o^2$ ---> $\omega_o = \frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{\frac{R1 + R3}{R2 + R3}} = \frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{\frac{rLf + re \cdot D \cdot D' + D'^2 \cdot R}{rCf + R}}$

Zin and Zo can be deducted the same way. To obtain the Vo/d AC transfer function, you can replace the PWM switch model by its small-signal equivalent and re-arrange the schematic until a known structure is found, exactly as we previously did. Discontinuous Conduction Mode (DCM) study would have required the use of the appropriate PWM switch model, but the principle remains the same.

SPICE simulations with the PWM switch model

Despite the fact that the PWM switch model was intended to be an alternative tool for teaching SMPS theory, the equivalent SPICE model lends itself very well to simulations. In his original form, the PWM switch model is only able to simulate an harmonic behavior. That is to say, you will have to provide the model with its DC operating points. For a BOOST operating in CCM, the DC parameters are shown in the box below. The INTUSOFT's IsSpice4 netlist of the PWM switch model in CCM is as follow:

```
.SUBCKT SWITCH          1 2 3 4 {D=0.45 VAP=11 IC=0.8}
*                       A P C Control
B1 7 1 V = { V(4)*(VAP/D) }
B2 1 2  I = { V(4)*IC }
B3 7 2  I = { I(Vd)*D }
B4 9 2 V = { V(7,2)*D }
Vd 9 3 0
.ENDS
```

BOOST DC PARAMETERS:
D={(VOUT-VIN)/VOUT}
VAP={-VOUT}
VAC={-VIN}
VCP={-VOUT+VIN}
IA={-((VOUT^2)/RL/VIN)*D}
IP={-VOUT/RL}
IC={-VOUT/RL/(1-D)}

If we now simulate figure 2b's schematic, we obtain the well-known second order response of a BOOST converter operating in CCM.

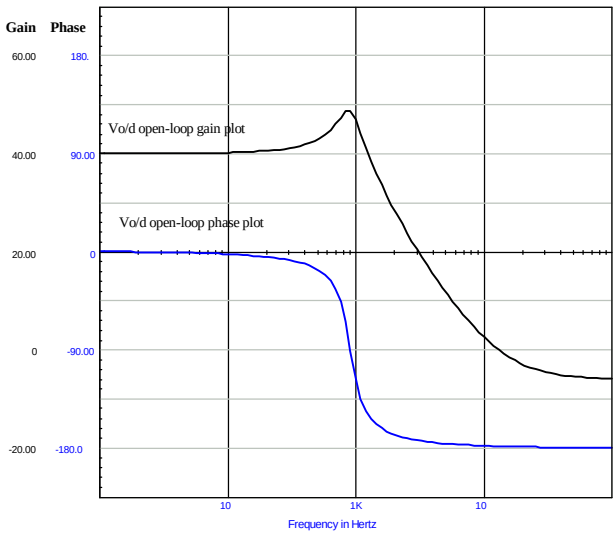
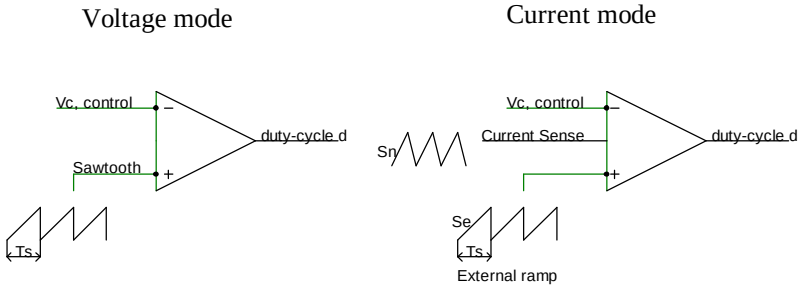


Figure 6

Current mode models

Numerous CMC models have been developed over the past decade. The first models suffered from their inability to predict the instabilities inherent to this kind of control. For instance, they were able to properly model the low frequency response of the CMC power stage, but the current-loop instability had to be addressed as a separate issue. In 1990, Raymond RIDLEY of VPEC, showed that a CMC power stage was best modeled by a third order polynomial form [6]. In his thesis, RIDLEY identified the current sampling action as being culprit of experimentally observed $F_{switching}/2$ sub-harmonic oscillations. Actually, a CMC differs from a voltage mode converter in the way the duty-cycle is generated. In **figure 7a**, the naturally sampled duty-cycle modulator is fed by an error voltage Vc and a reference sawtooth. This is classical voltage mode. **Figure 7b** depicts a current mode modulator where the current sense information is added, resulting in a different transfer function Fm for the Pulse Width Modulator section. Since the power stage was not affected by this change, RIDLEY built his model using the average PWM switch to which he added an internal current sampling loop.



$$Fm = \frac{d}{Vc} = \frac{1}{Se \cdot Ts}$$

Figure 7a

$$Fm = \frac{1}{(Sn + Se) \cdot Ts} = \frac{1}{m_c \cdot Sn \cdot Ts} \quad \text{where} \quad m_c = 1 + \frac{Se}{Sn}$$

Figure 7b

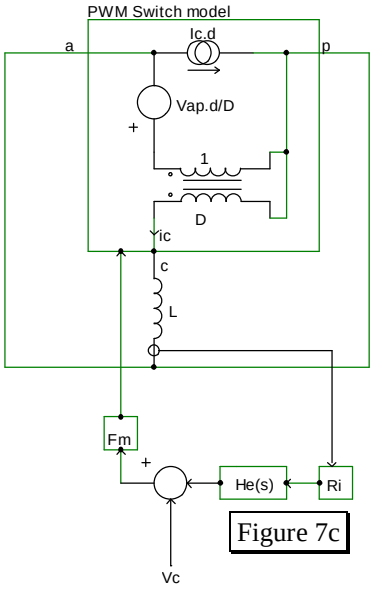


Figure 7c

The new model is presented in **figure 7c**, for steady-state on/off inductor voltages. He(s) is the second order polynomial form RIDLEY found to represent the sampling process in the continuous time, Ri scales the current information (delivered by a simple resistor or via a transformer) and Fm models the duty-cycle generation, as explained in **figures 7a** (Ri=0) or **7b** (Ri≠0). RIDLEY's model is universal since reducing Ri to 0 (or a very low value in IsSpice4) shadows the internal current loop and turn the model into voltage mode.

Current mode instabilities

A current mode controlled SMPS exhibits one low frequency pole, ω_p, and two poles which are located at Fs/2. These poles move in relation to the duty cycle and the external compensation ramp, when present. The two high frequency poles present a Q that depends on the compensating ramp and the duty cycle. RIDLEY demonstrated that the Q becomes infinite at D=0.5 with no external ramp, confirming the inherent instability of a current mode SMPS which has a duty cycle greater than 0.5. Q and ω_p, which are part of the V_o/V_c transfer function, are expressed as follows:

$$Q = \frac{1}{p \cdot (mc \cdot D' - 0.5)} \qquad \omega_p = \frac{1}{CR} + \frac{Ts}{LC} \cdot (mc \cdot D' - 0.5)$$

where $m_c = 1 + S_e / S_n$. S_e is the external ramp slope, S_n is the inductor on-time slope. D' = 1 - D

The presence of two high-frequency poles in the V_o/V_c transfer function is due to the sampling process of the inductance current. Actually, this process creates two RHP zeroes in the current loop which are responsible for the boost in gain at Fs/2 but also stress the phase lag at this point. If the gain margin is too low at this frequency, any perturbation in the current will make the system unstable since both voltage and current loops are embedded. You can fight the problem by providing the converter with an external compensation ramp. This will oppose the duty cycle action by lowering the current-loop DC gain and correspondingly

increasing the phase margin at Fs/2, which will damp the high Q poles in the V_o/V_c transfer function. As other benefits of ramp compensation, RIDLEY showed that an external ramp whose slope is equal to 50% of the inductor downslope could nullify the audio susceptibility (mc=1.5). As more external ramp is added, the low frequency pole ω_p moves to higher frequencies while the double poles will be split into two distinct poles. The first one will move towards lower frequencies until it joins and combines with the first low frequency pole at ω_p. At this point, the converter behaves as if it is operating in voltage mode (mc=32, **figure 8c**).

CMC models and IsSpice4

In his thesis report, RIDLEY presented his models in a simple SPICE2 format, without any parameter passing capability. The following IsSpice4 netlist provide greater flexibility by providing full SPICE3 parameter passing for the CCM model. The DCM listing will not be printed here but can be obtained via e-mail to the author at basso@esrf.fr.

```
.SUBCKT PWMCCM   1 2 3 4 5 {RI=0.33 L=37.5U FS=50K RL=1 D=0.45 VAP=11 VAC=6 IC=0.8 VP=2}
*                A P  C C' Control
.PARAM TS = {1/FS}              ; Switching time
.PARAM PI = 3.14159             ; PI constant
.PARAM KF = {-(D*TS*RI/L)*(1-D/2)}
.PARAM KR = {((1-D)^2*TS*RI)/(2*L)}
**** PWM Switch model ****
BE2 7 1 V = { V(17)*(VAP/D) }
BG1 1 2 I = { V(17)*IC }
BGxf 7 2 I = { I(Vxf)*D }
BExf 9 2 V = { V(7,2)*D }
Vxf 9 3 0
**** He(s) Circuit ****
Hi 10 0  Vxf  1
C1 10 12 {TS/PI}
L1 12 13 {TS/PI}
C2 13 14 {TS/PI}
Re 14 15  -1.57
E1 15 0 12 0 -1E6
**** Summing gains ****
BEd 16 0 V = { V(1,4)*KF + V(4,2)*KR + V(15)*RI + V(5) }
**** Modulator Gain ****
BEFm 17 0 V = { V(16)*1/(VP+(VAC*TS*RI/L)) }
.ENDS
```

BUCK DC parameters:
D={(VOUT/VIN)*(RL+RS)/RL} ; DC duty cycle for continuous mode
D={SQRT((M^2*8*L)/(((2-M)^2-M^2)*RL*(1/FS)))} ; Discontinuous mode
VAP={VIN}
VAC={VIN-VOUT}
VCP={VOUT}
IC={VOUT/RL}
IA={(VOUT/RL)*M}
IP={IC-IA}

As for the PWM switch, you need to provide the model with DC operating points. BUCK DC parameters are given above. You will notice the presence of the C' connection in the model. This connection is intended to inject current information inside the model, as reference [6] thoroughly explains.

A simple BUCK converter operating at 50kHz will be simulated, according to **figure 8a**.

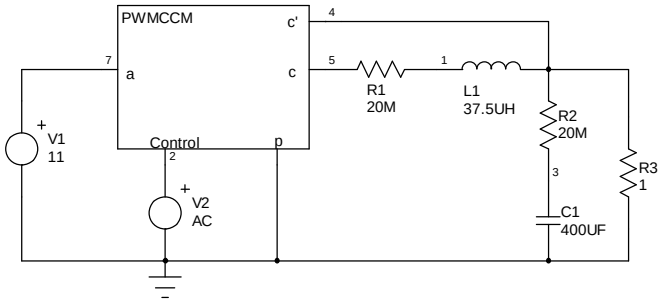
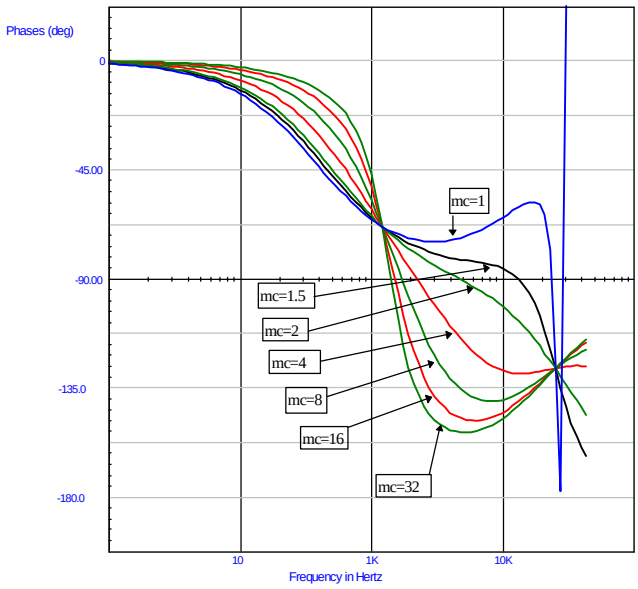


Figure 8a

The simulation results of **figures 8c** and **8d** clearly demonstrate the action of the compensation ramp upon the CMC BUCK converter. These curves have been automatically generated by IsSpice4 using its powerful Interactive Command Language in conjunction with the INTUSOFT's graphical investigation tool, IntuScope. For large mc (32), the converter's transfer function behaves like a classical voltage mode control system. Inversely, in lack of compensation ramp, the high Fs/2 Q will make the SMPS unstable in response to a transient step. The model would also let you investigate different transfer functions (audio susceptibility), Zin/Zout parameters and give an immediate insight of the compensation ramp effects.



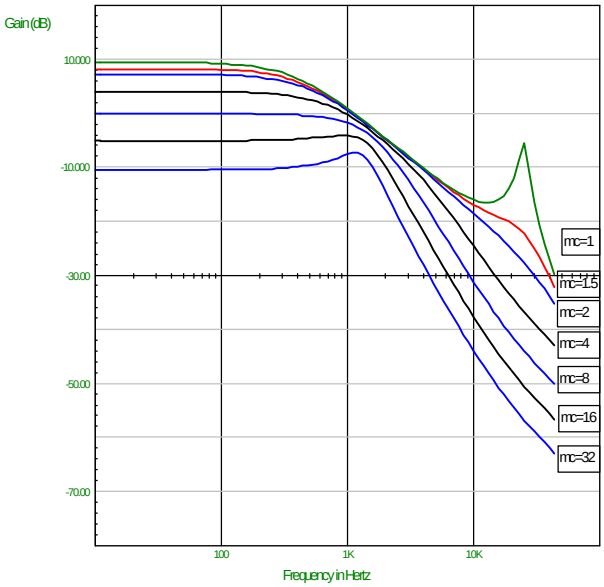


Figure 8b **Figure 8c**

New large-signal models

INTUSOFT has recently released its new SMPS library that contains numerous IsSpice4 models operating in switched or averaged mode. Among these novelties, the FLYAVG and FORWARD average models let you simulate any voltage/current mode converter and allow the testing to large steps. Reference [7] details the way the models were derived. As a simulation example, we will take figure 8a's BUCK converter to see how you can take profit of these new parts. **Figure 9a** depicts the electrical schematic whose netlist will be given to IsSpice4.

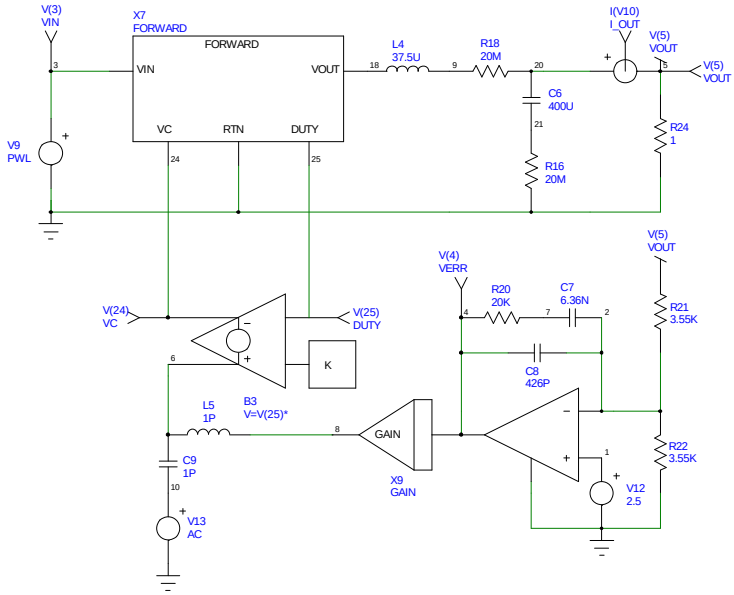


Figure 9a

The FLYAVG model does not take into account the previous Fs/2 high frequency poles. But it is well suited to study the impact of the compensation ramp upon the overall characteristics. For instance, RIDLEY showed an nullified audio susceptibility for an external ramp whose slope equals 50% of the inductor downslope. To highlight this phenomenon, let us sweep the K coefficient which sets the amount of external compensation in figure 9a. IsSpice4's optimizer capability will ease the work by providing the adequate

automation tool. You simply need to add the following line and run IsSpice4 to see multiple run results gathered upon a single graph (**figure 9b**): *OPT RAMP=0.1 TO 0.15 STEP=5M.

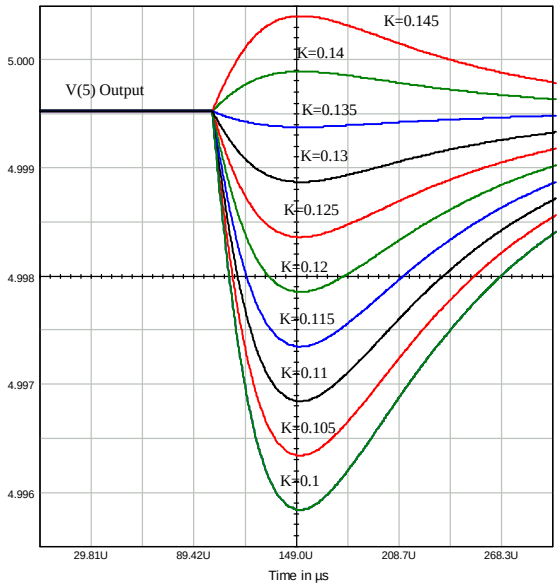


Figure 9b

For low compensation ramps, the phase of the line-to-output transfer function is negative. It is clearly depicted by the lower curves where the sudden stepped-up input voltage engenders a negative output transient. As more ramp is injected, the output step diminishes until null audio susceptibility is obtained, providing the designer with the value of the optimum ramp (K=0.135).

Conclusion

Both small and large-signal models should help the designer to better understand the intricacies of CMC converters stability. The new INTUSOFT's SMPS library includes averaged but also popular switched models (e.g UC384X family), giving the designer all the tools he needs to develop rugged designs from the theoretical study (average models) to realistic simulations (switched models).

References

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