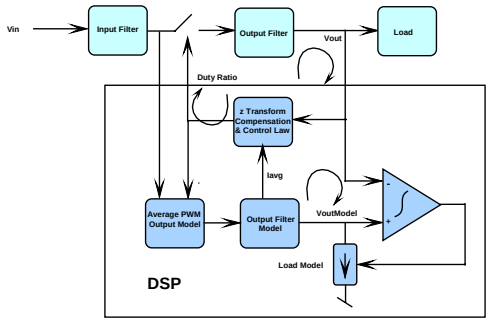
**Control Loops** Three control loops are identified in the Virtual Current Controller shown in Figure 1. The innermost loop controls duty ratio based on the plant models average current. Next the plant model estimates Load current based on matching actual output voltage with the predicted output voltage. Finally the outer loop controls the estimated current to provide a regulated output voltage. Designing these 3 loops requires opening the outermost loops while analyzing the inner loops. Doing this using a simulator is much easier than trying to accomplish the loop cuts in hardware. The simulator can actually give a bode plot of an unstable loop, allowing calculation of proper control system parameters without the destructive behavior of an oscillating power supply. Two basic concepts are used to make bode plots. First, a loop can be cut anywhere in this block by inserting a series voltage source, having an AC=1 value. Next, calling the forward direction Vin and the other side of the voltage source Vout, allows the IntuScope "b" script to make a bode plot. Here's the basics how the script works:

```
*&b Create a Bode, Hot key "b"
phase= phase(vout)-phase(vin)
plot phase
gain = db(vout) - db(vin)
plot gain
```

The real script is more complex, but the basic point is that IntuScope does the complex math for you. The loop is effectively cut using the voltage source, but the loop remains closed so that the operating points are correct. Next, opening the outer loops is done mathematically by adding high gain feedback in the AC analysis that nulls unwanted signal paths. A more detailed approach can be found studying the General Feedback Theorem, GFT and associated templates. SpiceNet schematic configurations are used to set up these loops, requiring the user to select the configuration from a drop down menu, run a simulation and press b in scope to get the bode plot. Figures 2,3 and 4 show the bode plots for the 3 loops.




**Block Diagram**

**Figure 1,** Virtual Current Control uses 3 Control Loops

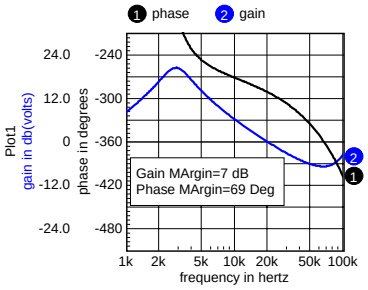



**Figure 1,** Inner Loop Margins

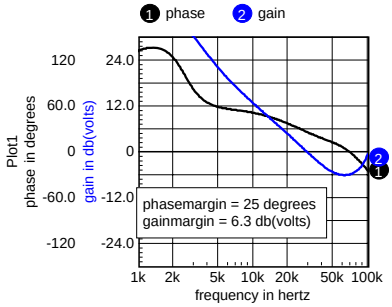



**Figure 3,** Plant Loop Margins

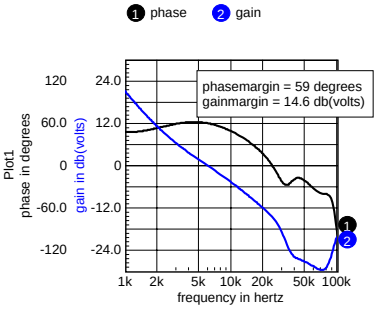



**Figure 4,** Main Loop Margins